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RELIABILITY HANDBOOK FOR SILICON MONOLITHIC MICROCIRCUITS

Volume 4 — Reliability Assessment of Monolithic Microcircuits

by Jim D. Adams, et al.

Prepared by
TEXAS INSTRUMENTS INCORPORATED
Dallas, Texas
for George C. Marshall Space Flight Center

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RELIABILITY HANDBOOK FOR

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FOREWORD

This handbook was prepared as an aid in determining the most effective application, testing, handling, and quality and reliability assurance controls for integrated circuits. It was compiled in two books of two volumes each and deals primarily with the subjects of application, failure mechanisms, failure analysis, and reliability assessment. Some similarity may be noted between NASA CR 1110, "Microelectronic Device Data Handbook," and the data presented herein; however, NASA CR 1110 deals with microcircuits in general, while this document was prepared as a reliability handbook and deals with monolithic microcircuits only.

The effort resulting in the publication of this handbook was produced under the technical direction of the Parts and Microelectronics Technology Branch, Future Programs and Technology Office, Quality and Reliability Assurance Laboratory, George C. Marshall Space Flight Center, Alabama.

D. Grau
Director, Quality and Reliability
Assurance Laboratory

PREFACE

This publication, "Reliability Assessment of Monolithic Microcircuits," is Volume 4 of a four-volume series entitled, "Reliability Handbook for Silicon Monolithic Microcircuits." The Handbook was prepared for the National Aeronautics and Space Administration by Texas Instruments Incorporated, under Contract NAS 8-20639. The Handbook series consists of the following volumes:

Volume 1 Application of Monolithic Microcircuits

Volume 2 Failure Mechanisms of Monolithic Microcircuits

Volume 3 Failure Analysis of Monolithic Microcircuits

Volume 4 Reliability Assessment of Monolithic Microcircuits.

The purpose of the Handbook is to provide aid in determining the most effective application and understanding of monolithic microcircuits, and the most effective quality and reliability assurance controls for the circuits.

Volume 4, "Reliability Assessment of Monolithic Microcircuits," describes:

- Failure rate information for each family of monolithic microcircuits, for operation at maximum rated conditions and at temperatures of 85°C, 55°C and 25°C.
- A curve that is used for extrapolation of failure rate at maximum rated conditions over the range from 0°C to 125°C.
- Where the failure rate of a specific monolithic microcircuit in one of the mentioned families is significantly different from the average for that family, the circuit and its failure rate are identified.
- Failure rates that are based on the latest available information; however, the use of acceleration factors has been avoided.

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VOLUME 4

RELIABILITY ASSESSMENT OF MONOLITHIC MICROCIRCUITS

GLOSSARY OF QUALITY AND RELIABILITY TERMS

Accelerated Test Conditions. Test conditions that are made more severe than recommended use conditions, to "accelerate" the occurrence of failures and, thus, shorten the test time required for reliability evaluations.

Acceptable Quality Level. The value of percent defective that a consumer indicates will be accepted most of the time by the acceptance sampling procedure to be used. (See "sampling plan.")

Acceptance Number. The largest number of defectives that can occur in a sample from an inspection lot and still permit the lot to be accepted.

Acceptance Sampling Plan. A procedure that specifies the number of units of product that are to be inspected (sample size or series of sample sizes), and the criteria for determining acceptability (acceptance and rejection numbers).

Acceptance Sampling. A procedure in which decisions to accept or reject are based on the examination of samples.

Acceptance Tests. Tests to determine conformance to design or specifications as a basis for acceptance. They may apply to parts, equipments, or systems.

Achieved Reliability. The system reliability demonstrated at a designated point in time.

Apportioned Reliability. An allocation of the overall numerical reliability requirement among each of the elements of a system.

Arithmetic Mean. See "average."

Assembly. A number of parts or subassemblies or any combination thereof joined together to perform a specific function.

Assurance. The relative confidence or certainty that specific program objectives will be achieved.

Attribute. A characteristic or property that a product either does or does not have; e.g., shorts and opens in electronic parts, leaks in hydraulic lines, dimensions of a machined tool or part, etc.

Attributes Testing. "Go-no-go" testing to evaluate whether a property does or does not fall within specification limits. The product is accepted if the property falls within these limits but is rejected if the product does not fall within them; the specific value of the property in either case is not measured.

Average. The arithmetic mean, the average of a set of n numbers, $X_1, X_2, \ldots X_n$, is the sum of the numbers divided by n, as follows:

$$\overline{X} = \frac{1}{n} \sum_{i=1}^{n} X_i \qquad (1)$$

Average Sample Number. The average number of sample units inspected per lot in reaching a decision to accept or to reject.

Binominal Distribution. A discrete random variable "X" has a binominal distribution if there exists $0 \leqslant p \leqslant 1$ and a positive integer n such that

$$P(X = x) = \binom{n}{x} p^{x} (1 - p)^{n - x} \tag{2}$$

where:

p = ratio of number of observed occurrences in "n" trials.

Breadboard Model. An assembly of preliminary circuits and parts to prove the feasibility of a device, a circuit, an equipment, a system, or a priniple in rough or breadboard form, without regard to the eventual overall design or form of the parts.

Catastrophic Failure. A sudden change—as opposed to a degradation or gradual change—in the operating characteristics of an item which renders the item useless in performing its design function.

Characteristic. A trait, property or quality of a specified item, type of item, or group of items.

Check-Out Time. Check-out time is that time required to determine whether the performance characteristics of a system are or are not within specified values.

Chi-Squared Function. A gamma function that expresses a distribution of many independent standardized variables. The form of the chi-squared function differs for each number of "degrees of freedom." Chi-squared is the sum of squares of independent normal variates divided by their common variance.

Component. A component is a combination of parts, which represents a self-contained element of a complete operating equipment, and performs a function necessary to the operation of that equipment. Examples: indicator unit, modulator unit, amplifier unit, etc.

Component and Part Reliability. A component or part is reliable when it will operate to a predetermined level of probability under its maximum electrical ratings at the most severe combination of environments for which it was designed, for the number of hours and duty cycle of the end equipment to which it is applied, without failures exceeding the rate tolerable to the satisfactory functioning of the end equipment.

Computed Reliability. The calculated probability of an item performing its purpose within specifications, based on estimates or tests of the reliability of its components.

Confidence Interval. A range of values that is believed to include with a preassigned degree of confidence (confidence level) the true characteristic of the lot or population, a given percentage of the time. For example, 95-percent confidence limits for a sample of 10 with a ratio of successes-to-total-number-of-items-tested of 0.9 (9 successes and 1 failure) would be 0.54 and 1.0. That is, even with an observed success ratio of 0.9 (90 percent), the best that can be said is that the true ratio lies between 0.54 (54 percent) and 1.0 (100 percent) as estimated 95 percent of the time.

Confidence Level. A statistical expression for the degree of desired trust or assurance in a given result. A confidence level is always associated with some assertion and measures the probability that a given assertion is true. For example, it could be the probability that a particular characteristic will fall within specified limits; i.e., the chance that the true value of P lies between P = a and P = b; a<b.

Confidence Limits. Extremes of a confidence interval within which the true value has a designated chance (confidence level) of being included.

Consumer's Risk. The risk, or probability, that a product will be accepted by some designated sampling plan test when it should be rejected.

Controlled Test. A test designed to control or balance out the effects of environmental differences and to minimize the chance of bias in the selection, treatment, and analysis of test samples.

Critical Defect. A defect that judgment and experience indicate could result in hazardous or unsafe conditions for individuals using or maintaining the product; a defect that could prevent performance of a specific function.

Debugging. A process of "shakedown operation" of a finished equipment performed prior to placing it in use. During this period, defective parts and workmanship errors are cleaned up under test conditions that closely simulate field operational stresses. The debugging process is not, however, intended to detect inherent weaknesses in system design. These should have been eliminated in the preproduction stages.

Degradation Failure. A failure that occurs as a result of a gradual or partial change in the characteristics of some part or parameter; e.g., drift in electronic part characteristics, changes in lubricant with age, corrosion of metal.

Derating. The technique of using a part, component, or equipment under stress conditions considerably below rated values, to achieve a "reliability margin" in design.

Distribution. See "statistical distribution."

Discrimination Ratio. A measure of steepness of the operating characteristics (OC) curve for an acceptance test between the acceptable quality level (AQL) and the lot tolerance percent defective (LTPD); i.e., the capability of the test to discriminate between "good" and "bad" product.

Downtime. The total time during which a system is not in condition to perform its intended function.

Early Failure Period. That period of life after final assembly, in which failures occur at an initially high rate because of the presence of defective parts and workmanship.

Environment. Aggregate of all the conditions and influences that affect the operation of equipments and components; e.g., physical location and operating characteristics of surrounding equipments and/or components; temperatures, humidity and contaminants of surrounding air; acceleration, shock and vibration; radiation; method of utilization; etc.

Environment Levels. Level of environment stresses created by operational conditions.

Equipment. One or more assemblies or a combination of units which independently perform a complete function.

Equipment Failure Rate. The ratio of the number of equipments that fail or malfunction (f) within a given period of time (t) to the total number of equipments (N) at the start of the test period; i.e., $\lambda = f/N$. This value is sometimes referred to as the hazard rate. A plot of the hourly hazard rate obtained from a life test and smoothed by means of a moving average will reveal the life characteristics of an equipment.

Equipment(s) Life. The arithmetic mean of cumulative operating time of identical equipments, beginning with acceptance by the ultimate consumer and ending at wearout.

Experimental Model. A model of the complete equipment that demonstrates the technical soundness of the basic idea. This model need not have the required final form or necessarily contain parts of final design.

Exponential Failure Law. An equipment is said to obey an exponential failure law if: 1) its failure rate, λ, is a constant or, equivalently, 2) its probability of surviving to time t without failure, R(t) is $e^{-\lambda t}$.

Exponential Distribution. For a random variable "x," the exponential distribution is defined as:

$$f(x) = \frac{1}{\theta} e^{-\frac{x}{\theta}} \tag{3}$$

where

$$\text{for } x,\ \theta > 0 \tag{4}$$

and

$$f(x) = 0 \tag{5}$$

elsewhere.

Exponentially Distributed. A series of observations ordered in time such that a constant rate of increase is shown over a long period. The general representation is the curve $y = ae^{bt}$, where a and b are constants. The distinguishing characteristic of an exponentially distributed probability function is "no memory," so that anything occurring in the next time interval between t and t + dt is not influenced by events earlier than time t.

Failure. The point at which an item fails to meet the minimum specified requirement essential to satisfactory performance. It occurs when equipment breaks down or when performance falls outside acceptable performance limits.

Failure Denisty Function. The failure density function f(t) represents the number of members of the original population being removed per unit time at t, divided by the number in the entire original population.

Failure Mechanism. That defect in material, workmanship, process, design, or test that was the ultimate cause of failure. It is that item that must be corrected to prevent further failures of the same type.

Failure Mode. The indicator, detector, or area of the part by which the failure was discovered. The basic relation between mode and mechanism is: the mode tells "how" a part failed, the mechanism tells "why" it failed.

Failure Rate. The expected number of failures in a given time interval. (For an exponential distribution of time-to-failure, the failure rate is equal to the reciprocal of the mean life.)

Failure Probability. The probability of failure in a specified period of time.

Gaussian Distribution. For a random variable x, the Gaussian distribution is defined by:

$$f(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{(x-\mu)^2}{2\sigma^2}} \tag{6}$$

where

$$-\infty < x < +\infty \tag{7}$$

Goal. A long-term requirement implied by specification or contract and used primarily for guidance. Goals are usually not legally binding because acceptance test requirements are not imposed.

Independent Failures. Those failures that occur or can occur without being related to the malfunctioning of associated items. In the development of the exponential failure law, it is essential to insure that each source of potential independent failure, which results in the complete malfunction of the equipment, be included.

Infant Mortality. Early failures occurring at a rate substantially greater than that observed during subsequent life prior to wearout. Infant mortality may be reduced by stringent quality control and appropriate screening.

Inherent Reliability. The degree of reliability built into a product because of design and development.

Initial Failure. The first failure to occur in a specified period of time.

Inspection of Attributes. An inspection wherein the unit of production is classified simply as defective or nondefective with respect to a given requirement or set of requirements. If desired, the degree of nonconformance may be further categorized through the use of such classifications as critical, major, and minor.

Inspection by Variables. An inspection wherein a specified quality characteristic of a unit of product is measured on a continuous scale, such as pounds, inches, or feet-per-second, and a measurement is recorded; or an inspection wherein certain characteristics of the sample units are evaluated with respect to a numerical scale and are expressed as precise points along this scale. The

distribution of these points, as established by measures of their central tendency and dispersion, are mathematically related to specified requirements to determine the degree of conformance of the characteristics.

Inspection Level. A term used to indicate the number of sample units required for inspection of a given amount of product. All other things being equal, a higher inspection level entails a lower risk of acceptance of a lot of inferior quality, and a lower inspection level entails a higher risk.

Inspection Lot. A collection of units of product manufactured or processed under substantially the same conditions and offered for inspection at one time, or during a fixed period of time.

Interchangeability. The ability to interchange, without restriction, life equipments or portions thereof in manufacture, maintenance, or operation.

Interfaces. Boundary conditions and requirements existing between two or more "mating" subsystems or components; e.g., impedance matching, structural fitting, thermal and vibration levels.

Life Characteristic. Relation between the failure rate of equipment and operating or test time. When the design provides adequate stress safety factors, the most frequent failure characteristic will be a random failure rate that is inherent in the part reliability capabilities.

Logistic Downtime. That portion of downtime during which repair is delayed solely because of the necessity for waiting for a replacement part or other subdivision of the system.

Longevity. Length of life to wearout.

Lot Tolerance Percent Defective. The percent defective for each lot that the sampling plan will accept 10 percent of the time.

Maintainability. The probability (when maintenance action is initiated under stated conditions) that a system will be restored to its specified operational condition within a specified period of downtime.

Major Defect. A defect that reduces the useability of the product for its intended purpose.

Malfunction. A general term used to denote the occurrence of failure of a product to give satisfactory performance. A malfunction need not constitute a failure if readjustment of operator controls can restore an acceptable operating condition.

Marginal Testing. A procedure for system checking that indicates when some portion of the system has deteriorated to the point where there is a high probability of a system failure during the next operating period.

Mean Life. The arithmetic average of population life.

Mean-Time-Between-Failures. The total measured operating time of a population of equipments divided by the total number of failures. The measured operating time of the equipments of the population which did not fail must be included. This measurement is normally made during that period of time between the early life and wear-out failures. In the case of exponential distribution of time between failures, this ratio is the reciprocal of failure rate. The mean-time-between-failures

(MTBF) can be determined by dividing the product of the number of equipments tested (N) and the test time (t) by the number of failures (n) which occur during that time, i.e., MTBF or often just M = Nt/n. "M" is the reciprocal of failure rate (λ); i.e., $M = 1/\lambda$, and is related to the probability of survival of the exponential law as follows:

$$P_s = e^{-t/M} = e^{-\lambda t} \tag{8}$$

Mean-Time-To-Failure. The average length of time to failure of nonrepairable items; i.e., the total operating time under specified conditions divided by the number of failures during this time (in the exponential case, the mean-time-to-failure is the reciprocal of the failure rate per unit time).

Mean-Time-To-Repair. A measure of repairability, expressed as the total repair time over a specified period divided by the total repairs made during that period.

Minor Defect. A minor defect is one that does not materially reduce the usability of the unit of product for its intended purpose, or, is a departure from established standards having no significant bearing on the effective use or operation of the unit.

Multiple Sampling. Sampling inspection in which, after each sample is inspected, the decision is made to accept, to reject, or to take another sample, but in which there is a prescribed maximum number of samples, after which, decision to accept or to reject must be reached.

Normal Distribution. See "Gaussian Distribution."

Operating Characteristic Curve. The quality curve which shows for a particular sampling plan the relation between 1) the fraction defective in a lot, and 2) the probability that the sampling plan will accept the lot.

Operating Reliability. The probability that a system or unit will give satisfactory performance for a given period when used in the manner and for the purpose intended. "Operating Reliability" consists of the inherent reliability as degraded by various application factors peculiar to each field condition.

Part. A unit which is not normally subject to disassembly without destruction of designed used.

Part Stress. Those factors of usage (or test) which tend to affect the failure rate of parts. These include voltage, power, temperature, and frequency.

Parameter. A quality or value that remains constant within a given set of conditions; i.e., is subject to change only if the conditions change.

Poisson Distribution. A discrete random variable "x" has a Poisson distribution with mean $m>0$ if:

$$P(x = k) = \frac{m^k e^{-m}}{k!} \tag{9}$$

where

$$k = 0, 1, 2, \ldots\ldots\ldots\ldots\ldots\ldots \tag{10}$$

Population. The total collection of units from a common source. The conceptual total collection of units from a process, such as a production process. Also used in the sense of a "universe (or population) of observation." The terms "universe," "population," and "parent distribution" are synonymouns. (Statistical quality control is based on distributions in the population domain as contrasted to the time domain for reliability.)

Probability. The limiting relative frequency in an infinite random series. If an event can occur in "n" ways and fail in "m" ways, and if these m + n ways are equally likely, then the mathematical probability that the event will occur in any one trial is the ratio n/(n + m). The probability of an event is the theoretical relative frequency with which it will occur, such relative frequency being the ratio of the number of times the event is observed under experimental conditions to the total of a great number of observations made under those same conditions.

Probability Limits. Upper and lower limits assigned to estimated value to indicate the range within which the true value is supposed to lie according to some statement of a probabilistic character.

Probability of Acceptance. The probability that a lot or process will be accepted.

Probability of Survival. The likelihood of an item performing its intended function for a given period of time or number of duty cycles, measured by the ratio of the number of survivors at time, t, to the population at the beginning of the period.

Producer's Risk. The risk or probability that a product will be rejected by test, when it should properly be accepted.

Qualification Test. Such testing of a product as may be necessary to determine whether or not the product conforms to qualification requirements in the applicable specification.

Quality Characteristics. Those properties of an item or process that can be measured, reviewed, or observed, and that are identified in the drawings, specifications, or contractual requirements. Reliability becomes a quality characteristic, when so defined.

Random Failure. Any failure which occurs by chance, in an accidental, casual, or haphazard manner. Random failures may or may not be related to known failure modes.

Randomness. An equal chance for any of the possible outcomes.

Random Sample. A random sample is one in which each item in the lot has an equal chance of being selected in the sample.

Redundancy. The existence of more than one means for accomplishing a given task, where all means must fail before there is an overall failure in the system. Parallel redundancy applies in systems where both means are working at the same time to accomplish the task, and either of the systems is capable of handling the job itself in case of failure of the other system. Standby redundancy applies to a system where there is an alternate means of accomplishing the task, that is switched in by a malfunction sensing device when the primary system fails.

Rejection. An action indicating nonacceptance of material. In most cases material is rejected as being nonacceptable with regard to certain features, with the understanding that upon correction, the material may be resubmitted for inspection and acceptance.

Reliability. The probability of performing, without failure, a specified function under given conditions for a specified period of time.

Reliability Life Test. Testing of a sample under specified conditions for predetermined periods of time or until a predetermined number of failures has occurred, for the purpose of estimating the mean-time-to-failure or mean-time-between-failures at a specified confidence level.

Reliability Operating Characteristic Curve. The operating characteristic of a reliability acceptance test.

Regression Analysis. An analytical method for determining the correlation between several variables.

Repair Rate. A measure of repair capability; i.e., number of repair actions completed per hour (reciprocal of mean-time-to-repair in the exponential case).

Repairability. The probability that a failed system will be restored to operable condition within a specified active repair time.

Risk. The probability of making an incorrect decision.

Sampling Plan. A specific plan that states 1) the sample size and 2) the criteria for accepting, rejecting, or taking another sample.

Screen, Hi-Rel. A scheme whereby marginal (weak) items are eliminated from a lot through the use of additional environmental stresses such as temperature cycling, centrifuge, electrical operation at high stress levels, etc. The end goal of screening is to reduce to a minimum the incidence of infant mortality in the final product.

Sequential Test. A test of a sequence of samples in which it is decided at each step in the sequence whether to accept or reject the hypothesis, or to take an additional sample and continue the test.

Specification. A detailed description of the characteristics of a product and of the criteria which must be used to determine whether the product is in conformity with the description.

Shelf Life. Storage or nonoperational time that can be accumulated on equipment before it is placed in operating use.

Standard Deviation. The positive square root of the second moment about the mean; analogous to radius of gyration. The standard deviation (usually denoted by σ) of a random variable (and of its distribution) is the square root of its variance. The standard deviation of a set of "n" numbers X_1, X_2, ...X_n is the root-mean-square (rms) deviation of the numbers from their average:

$$\sigma = \sqrt{\frac{\sum_{i=1}^{n} (x_i - \bar{X})^2}{n-1}} \qquad (11)$$

Statistical Distribution. A mathematical relationship that describes a particular behavior pattern exhibited by some common characteristic of a group of items drawn from a homogeneous population.

Stress Analysis. The evaluation of stress conditions (electrical, thermal, vibration, shock, humidity, etc.) under which parts are applied in the design of a system or equipment. On the basis of a stress analysis, failure rates are appropriately adjusted to reflect the deleterious effects of the stress on the reliability of the parts involved.

Subassembly. Two or more parts that form a portion of an assembly, or form a unit replaceable as a whole, but having a part or parts that are replaceable as indivduals.

Subsystem. A major subdivision of a system that performs a specified function in the overall operation of a system.

Support Equipment. Items that are necessary for the operation and/or maintenance of the system but are not physically part of the system.

System. A combination of complete operating equipments, assemblies, components, parts, or accessories that are interconnected to perform a specific operational function.

System Compatibility. The ability of the equipments within a system to work together to perform the intended mission of the system. In a broader sense, system compatibility is the suitability of a system to provide the levels of field performance, reliability, and maintainability required by the military services.

Test to Failure. The process of subjecting an item to successively increasing stress levels until failure occurs. Commonly known as step stress testing.

Thermal Survey. The prediction or actual measurement of part ambient temperatures to detect the existence of "hot spots" and to determine the need for cooling.

Truncation. Deletion of portions of a distribution greater than or less than a certain value. Truncation of a sequential test means termination of the test prior to reaching a decision under the sequential plan.

Unreliability. Probability of failure for a given time under specified environments. The difference between the equipment reliability and unity.

Uptime. The time in which a system is in condition to perform its intended function.

Useful Life. The total operating time between debugging and wearout.

Variables Testing. A test procedure wherein the items under test are classified according to quantitative rather than qualitative characteristics. Variables testing yields more information than attributes testing.

Wear-Out. The point at which further operation is uneconomical.

Wear-Out Failures. Those failures which occur as a result of deterioration processes or mechanical wear and whose probability of occurrence increases with time.

Wear-Out Period. The wear-out period of an equipment is that period of equipment life, following the normal operating period, during which the equipment failure rate increases above the normal rate.

VOLUME 4
RELIABILITY ASSESSMENT OF MONOLITHIC MICROCIRCUITS

SECTION I

INTRODUCTION

The basic answer to, "What reliability can I expect from my equipment, using monolithic microcircuits?" is indeed a complex one. The purpose of this Volume 4 of the Handbook is to give a system designer or user basic information which will allow him to answer the question posed.

It should be strongly noted that the responsibility for this final system reliability is a shared one between the manufacturer and user. However, the more thoroughly the basic device and its intended use are understood, the more clearly this responsibility can be identified.

SECTION II

DEFINITION OF RELIABILITY

A. REVIEW OF BASIC RELIABILITY STATISTICS AND DEFINITIONS

1. General

The areas of reliability and quality control are often avoided by engineers and scientests not intimately associated with these functions. This is understandable because when one first enters these areas he is confronted by a totally new and unique language that is, to say the least, confusing. Terms such as Lambdas, LTPD's, AQL, percent/1000 hours, MTBF, etc. are unique to quality and reliability engineering. In order to understand the material presented in the following sections of this Volume of the Handbook, it will be necessary for the reader to have a good understanding of the concepts and terms about which the discussion is formulated. A glossary of the most commonly used terms is located in the preface of this volume. The discussion presented here will describe basic concepts and models frequently used in quality and reliability engineering.

2. Quality Concepts

a. General

Quality may be defined as a product's degree of conformance to specified characteristics. The degree of conformance is agreed upon by both producer and user and is administered through the use of a sampling plan which is in itself a method of operation or procedure.

Quality must be inherent to a product. That is, it is not possible to achieve quality through the performance of inspections and tests alone. It should be noted that "defective product" can be "screened out" by proper tests, and the result will be that only the good product will be used. The point is that these tests do not improve the status of the material that was good at the beginning. A quality product demands:

- Careful specification and continuous control of input materials.
- A manufacturing process defined by specification.
- Continuous "in-process" control.
- Final quality product acceptance to insure conformance to customer specifications.

The assessment of product quality is accomplished through the use of sampling plans. Sampling plans may be designed to virtually any degree of protection required by the customer. The

choice is an economic consideration involving inspection costs and costs associated with the user placing a defective unit in his product. For any given situation there is a balancing of economic considerations where the law of diminishing returns goes into effect with respect to manufacturing re-work costs, cost of inspection, and the cost of that portion of acceptable product that is rejected.

b. Measurement of Protection Afforded by a Sampling Plan

Acceptable Quality Level. The percent of defective devices which for the purposes of acceptance sampling can be considered satisfactory as a process average is referred to as "acceptable quality level" (AQL). A group of devices that contains a defect percentage that is equal to the AQL has a high probability of being accepted. From the consumer's point of view, the ideal level would be that at which no defectives are allowed. However, the cost of attaining and maintaining such a level may not be economical for the user. Frequently used AQL levels range from 0.4 percent to 6.5 percent defective devices, depending upon the critical nature of the product.

Lot Tolerance Percent Defective. The percent defective for each lot (a number of units of an article offered as one item) that the sampling plan will accept 10 percent of the time is the "lot tolerance percent defective" (LTPD). Typical values of LTPD range from 5 percent to 10 percent, depending upon use conditions. The final quality specifications arrived at between manufacturer and consumer is, therefore, an economic balance between perfect quality (0 percent defective) and conditional limitations. The method most commonly employed to evaluate lot quality is based on statistical principles of random samples selected from a lot. The entire lot is evaluated (i.e., accepted or rejected) on the basis of the selected sample's ability to satisfy the established criteria. The criteria is such that good quality material will be accepted most of the time and inferior quality material will be rejected most of the time. This is not to imply, however, that sampling is the only method used; many high reliability applications require the use of 100 percent inspection. (The efficiency of "100-percent" inspections must be understood before it is assumed that a 100-percent inspection can yield better than sampling results.)

Operating Characteristics Curve. The selected sampling plan is defined by its Operating Characteristics Curve (OC curve), as illustrated in Figure 4-1. The OC curve is a graphical presentation of the probability that a lot of a given quality will be accepted. The horizontal axis represents the lot quality, and the vertical axis represents the probability of acceptance. Two points on this curve are of utmost importance to the manufacturer and consumer; they are defined as "producer's risk" and "consumer's risk."

The "producer's risk" is the statistical chance that the sampling plan will cause the rejection of a lot which is actually of acceptable quality. This risk is usually established at 5 percent, that is, there is a 95-percent chance that a lot of satisfactory quality will be accepted. The satisfactory quality, in terms of percent defective allowable, is assigned to this point and is called the "acceptable quality level" (AQL).

There is a statistical chance that the sampling plan will permit the acceptance of a lot which is actually of unacceptable quality. This statistical chance is the consumer's risk and it is usually established at 10 percent, that is, there is 10-percent chance that a lot of unacceptable quality will

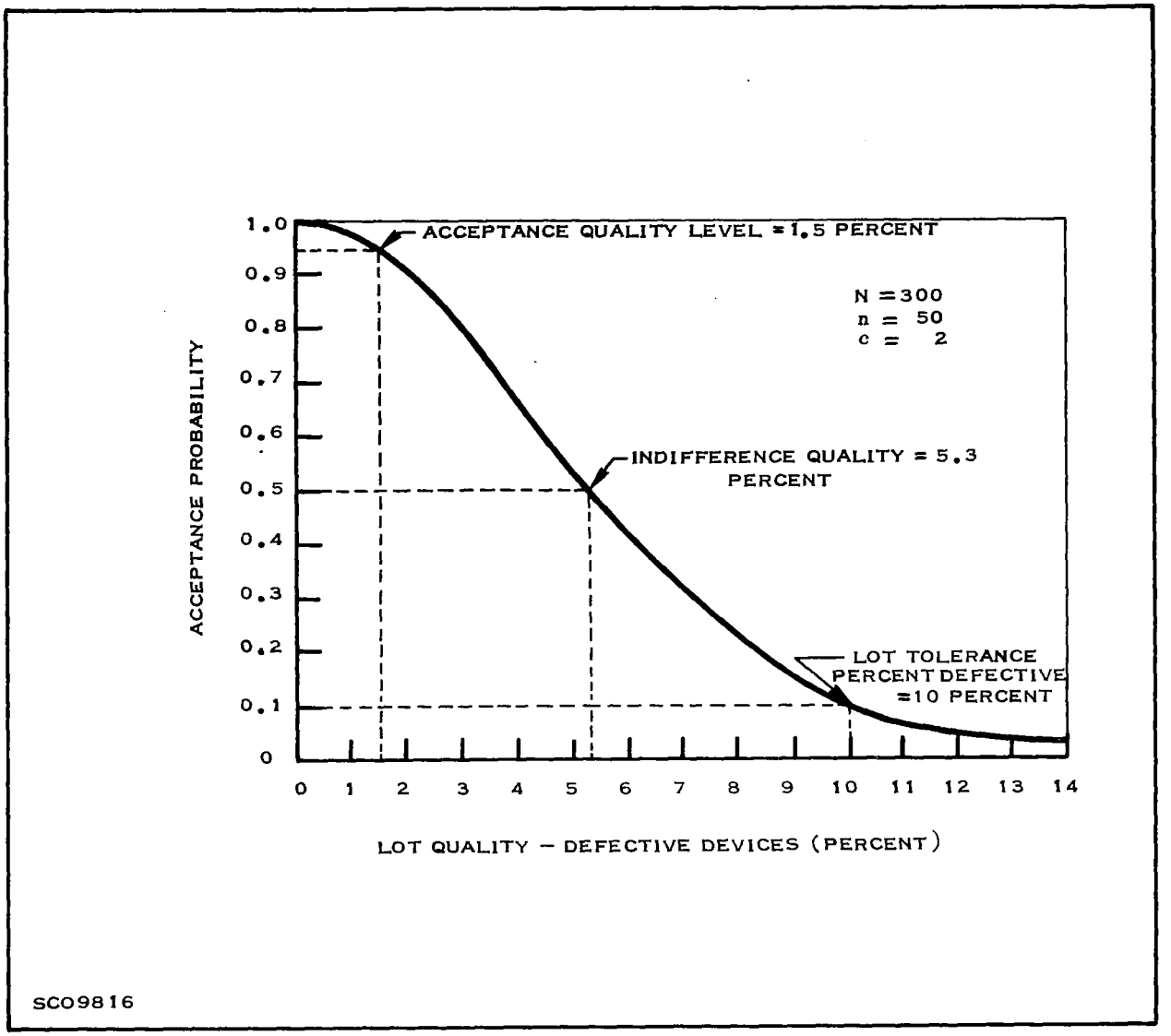

Figure 4-1. Operating Characteristic Curve

be accepted. The unacceptable quality, in terms of percent defective, is assigned to this point and is called the "lot tolerance percent defective" (LTPD).

In Figure 4-1, the AQL is 1.5 percent defective, and the LTPD is 10 percent defective. The probability of accepting a lot of any other quality may be read from the curve. The lot quality which will be accepted as often as it will be rejected is termed "indifference quality" and it occurs at the 50 percent probability point of acceptance. For the sampling plan of Figure 4-1, the indifference quality is 5.3 percent defective.

Average Outgoing Quality Curve. "Average outgoing quality" is another criteria of the protection afforded by a sampling plan. Lots that have been rejected may be returned to the manufacturer as unacceptable, with no further action required. However, an often more desirable

approach is to submit rejected lots to screening, and then to replace all defective units with good units. The screening may be performed by either the consumer or the manufacturer. Usually, the manufacturer performs the screening because of economic considerations (test equipment, manpower, etc.) Using this approach, the average quality going out of inspection is a function of quality supplied.

As an example, a number of lots, each of which is 3 percent defective, are received at the incoming inspection activity. Using the curve of Figure 4-1, 80 percent will be accepted and stocked at 3 percent defective. The remaining 20 percent of the lots will be rejected, scanned, and returned to stock as 0 percent defective (perfect screening is assumed). For an incoming quality of 3 percent defective, an "average outgoing quality" (AOQ) of 2.4 percent [(0.03 · 0.80) + (0.00 · 0.20) 100] defective is realized.

It is customary to calculate AOQ for various levels of incoming quality and thereby generate the AOQ curve of Figure 4-1. This curve reaches a maximum point which is termed the "average outgoing quality limit" (AOQL). Thus, when incoming lot quality is perfect, outgoing lot quality is also perfect. However, when incoming lot quality is extremely poor, outgoing lot quality will be near perfect, since the sampling plan will cause rejection of such lots by subsequent screening and removal of defective material. The AOQ curve for the described sampling plan described is shown in Figure 4-2. For this plan the AOQL is 2.7 percent defective and occurs when the incoming material

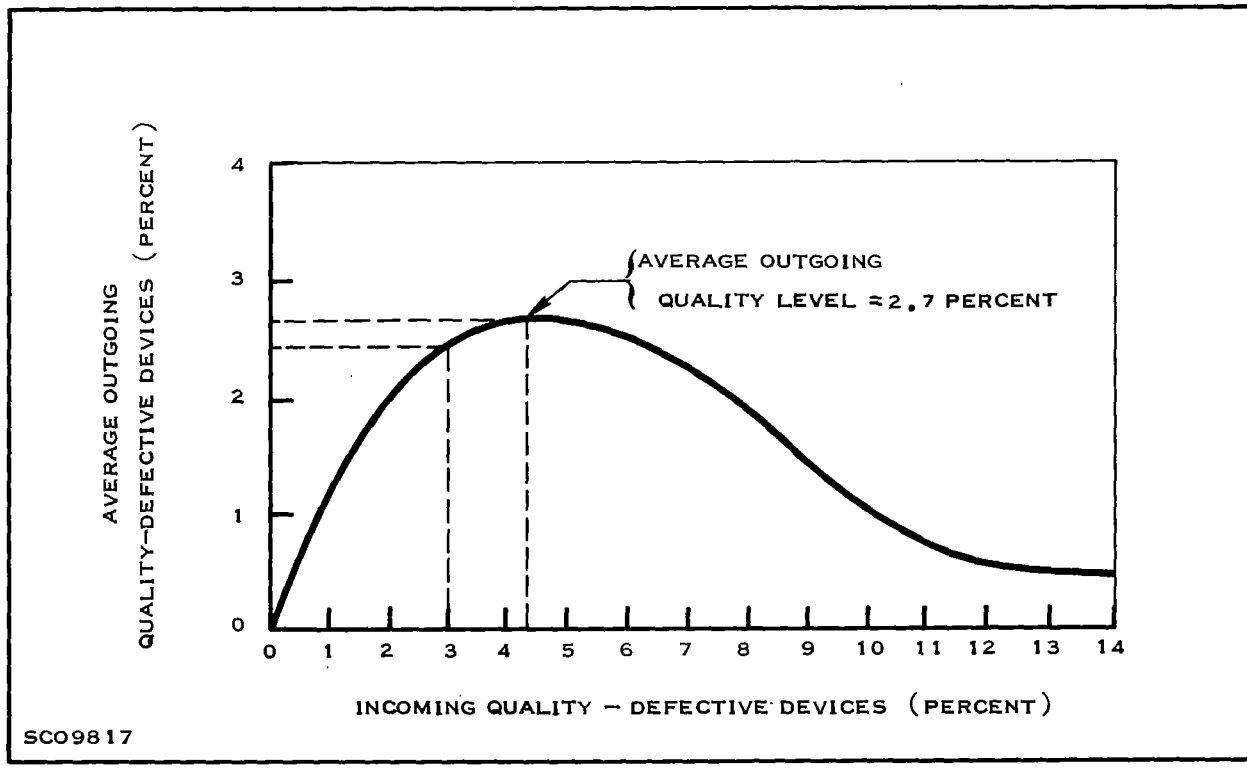

Figure 4-2. Average Outgoing Quality Curve

quality is 4.3 percent defective. Also plotted in Figure 4-2 is the previously mentioned AOQ point of 2.4 percent defective.

Sampling Plan. A sampling plan is usually specified with three numbers: the lot size (N), the sample size (n), and the acceptance number (c). The sampling plan described by the OC curve of Figure 4-1 shows that from a lot of 300 units, a sample of 50 units is to be selected at random, and that upon completion of sample inspection the lot is to be accepted if 2 or less defective units are found.

The merits of a particular sampling plan are illustrated by its OC and AOQ curves and the selected curve points of AQL, LTPD, AOQL, and "indifference quality." A change in lot size (N), sample size (n), or acceptance number (c), will result in a change in shape of the original OC curve. In general, a change in lot size will alter the OC curve to a very small extent, and the AQL and LTPD points will remain virtually unchanged. This change is particularly small when the sample represents less than 10 percent of the lot. A change in sample size will result in an OC curve with a different slope. An increase in sample size results in a curve with a sharper slope and hence moves the LTPD point closer to the AQL point. An increase in the acceptance number shifts the OC curve to the right along the horizontal axis. This shift in the OC curve results in increases in AQL and LTPD.

All comments thus far have been in reference to single sampling plans, that is, where single samples of units are observed. Double and multiple sampling plans also exist and are used. Double sampling involves the selection of a sample from a lot and, under defined circumstances, the selection of a second sample before accepting or rejecting the lot. As the name implies, multiple sampling involves the selection of multiple samples before rendering the acceptance or rejection decision.

Double sampling plans permit a smaller first sample than that of corresponding single sample plans. When the percent defective of submitted material is either low or high, it is often possible to accept or reject lots based upon the first sample. However, when the percent defective of submitted material is near the acceptable quality level, single sampling plans frequently require the inspection of fewer units than will comparable double sampling plans. In practical applications, the grater complexity of multiple sampling plans often overshadows the benefits of reduced total units inspected.

The important point is that the inspection decision is fully determined by lot size, sample size, and acceptance number. In addition, the sampling plan is governed by its OC curve and the associated merit points previously discussed. The following is a comparison of the relative merits of single, double, and multiple sampling plans with respect to some of the parameters of sampling plans:

- Acceptance in Use:
    - Single sampling—one chance to arrive at acceptance/rejection decision.

  - Double sampling–possibility of required second sample before acceptance/rejection decision can be made.
  - Multiple sampling–often termed indecisive because of frequently incurred multiple samples.
- Number of Units Inspected per Lot:
  - Single sampling–generally highest.
  - Double sampling–generally (but not always) 15 to 40 percent less than single sampling. Total units inspected is dependent on incoming percent defective.
  - Multiple sampling–generally (but not always) less than double sampling, by approximately 25 percent. Total units inspected is dependent on incoming percent defective.
- Sampling Plan Administrative Cost (this includes training, personnel, records, sample identification, handling, etc.):
  - Single sampling–lowest cost.
  - Double sampling–greater than for single sampling.
  - Multiple–highest.
- Quality Information Obtained (this concerns validity of information pertaining to lot quality):
  - Single sampling–most information to assess lot quality.
  - Double sampling–less than for single sampling.
  - Multiple sampling–least information.

Sampling Plan Applications. At present, two methods are in common use for the specification of sampling plans. The first relates to the specifying of AQL values, while the second involves the specifying of LTPD values along with maximum acceptance numbers. The former specifies the producer's risk, while the latter specifies the consumer's risk. Each has its own merits, and a given sampling plan can best be evaluated from its OC curve so that both producer and consumer can properly evaluate their individual risks.

The document frequently used in the selection of AQL-type sampling plans is MIL-STD-105. A chart of single sampling plans based upon data extracted from this document is shown in Table 4-1. Charted are plans for lot sizes from 2 to 3200 for AQL's from 0.40 percent defective to 6.5 percent defective. The acceptance number (c) and LTPD in percent defective is given for each value of AQL.

This portion of the discussion will serve to illustrate the use of Table 4-1. A lot consisting of 175 microcircuits is to be evaluated for specific characteristics to an AQL of 0.40 percent defective. From the chart, a sample of 32 devices is selected at random. The acceptance number is 0 (no defective devices) and the LTPD or consumer's risk is 6.9 percent defective.

Table 4-1. Single Sampling Plans for Normal Inspection (for Lot Sizes 2 to 3200 and AQL's from 0.40 to 6.5)

Lot Size (N)	Sample Size (n)	Acceptable Quality Level (AQL)													
		0.40		0.65		1.0		1.5		2.5		4.0		6.5	
		c	LTPD	c	LTPD	c	LTPD	c	LTPD	c	LTPD	c	LTPD	c	LTPD
2 to 8	2													0	68
9 to 15	3											0	54		
16 to 25	5									0	37				
26 to 50	8							0	25					1	41
51 to 90	13					0	16					1	27	2	36
91 to 150	20			0	11					1	18	2	25	3	30
151 to 280	32	0	6.9					1	12	2	16	3	20	5	27
281 to 500	50					1	7.6	2	10	3	13	5	18	7	22
501 to 1200	80			1	4.8	2	6.5	3	8.2	5	11	7	14	10	19
1201 to 3200	125	1	3.1	2	4.3	3	5.4	5	7.4	7	9.4	10	12	14	16

Note: Use first sampling plan below arrow. If sample size equals or exceeds lot size, do 100% inspection

Use first sampling plan above arrow.

The document frequently used for the selection of LTPD type sampling plans is MIL-S-19500. The data shown in Table 4-2 herein were extracted from Table C-I of MIL-S-19500 and are the minimum sample sizes required to insure an LTPD (at consumer's risk) not greater than that specified. The table covers LTPD values of 2-to-30 percent for acceptance numbers from 0 to 10. The data are valid for lot sizes greater than 200. For example, a sample of 38 is required to insure an LTPD of 10 percent with an acceptance number of 1, and a sample of 77 is required to insure an LTPD of 5 percent with the same acceptance number.

Table 4-2. Sampling Plans for Lot Sizes Greater than 200*

Acceptance Number	LTPD							
	30	21	15	10	7	5	3	2
	Minimum Sample Size†							
0	8	11	15	22	32	45	76	116
1	13	18	25	38	55	77	129	195
2	18	25	34	52	75	105	176	266
3	22	32	43	65	94	132	221	333
4	27	38	52	78	113	158	265	398
5	31	45	60	91	131	184	308	462
6	35	51	68	104	149	209	349	528
7	39	57	77	116	166	234	390	589
8	43	63	85	128	184	258	431	648
9	47	69	93	140	201	282	471	709
10	51	75	100	152	218	306	511	770

*May be used for lot sizes of 200 or less, with tighter LTPD values than those given.

†Minimum sample size to insure with 90 percent confidence an LTPD not greater than that specified.

Sampling plans for lot sizes of 200 or less are included in Tables 4-3, 4-4, and 4-5. These three tables are based on acceptance numbers 0, 1, and 2, respectively. Comparison Tables 4-2, 4-3, 4-4 and 4-5 shows that Table 4-2 may be used for sampling lots of less than 200. When this is done, the result is that the insured LTPD will be tighter than that originally specified. Use of Tables 4-3, 4-4 and 4-5 will be illustrated by an example.

Table 4-3. Hypergeometric Sampling Plans for Lot Sizes of 200 or Less (Acceptance Number = 0)

Sampling Size	Lot Size 10	20	30	40	50	60	80	100	120	150	160	200
	LTPD at 10 percent Acceptance Probability for Zero Failures											
2	65	66	67	67	67	68	68	68	68	68	68	68
4	36	40	42	42	42	43	43	43	43	43	44	44
5	29	33	34	35	35	35	36	36	37	37	37	37
8	15	20	22	23	23	23	24	24	24	24	24	25
10		15	17	19	19	19	20	20	20	20	20	20
16		6.9	10	11	11	12	12	13	13	13	13	13
20			6.8	8.0	8.7	9.0	9.4	10	10	10	10	11
25			4.3	5.7	6.4	6.9	7.4	7.5	7.6	7.7	7.8	7.9
32				3.7	4.4	5.0	5.5	5.9	6.0	6.2	6.3	6.3
40					3.0	3.4	4.0	4.5	4.6	4.9	5.0	5.0
50						2.3	2.9	3.3	3.5	3.7	3.7	3.9
64							1.7	2.2	2.5	2.7	2.8	2.9
80								1.5	1.7	2.0	2.1	2.2
100									1.1	1.5	1.5	1.7
125										0.8	0.9	1.2
128										0.8	0.9	1.1
160												0.7

Table 4-4. Hypergeometric Sampling Plans for Lot Sizes of 200 or Less (Acceptance Number = 1)

Sampling Size	Lot Size 10	20	30	40	50	60	80	100	120	150	160	200
	LTPD at 10 percent Acceptance Probability for One Failure											
2	95	95	95	95	95	95	95	95	95	95	95	95
4	62	66	66	67	67	67	67	67	67	67	67	68
5	51	55	56	57	57	58	58	58	58	58	58	58
8	28	35	38	38	39	39	39	39	39	40	40	40
10		30	30	31	32	32	32	33	33	33	33	33
16		15	18	18	20	20	21	21	21	21	22	22
20			13	15	16	16	16	16	17	17	17	18
25			9.2	11	12	13	13	13	13	14	14	14
32				7.4	8.2	9.0	9.9	10	10.4	11	11	11
40					5.9	6.8	7.6	7.8	8.2	8.3	8.4	8.6
50						4.6	5.6	6.1	6.4	6.5	6.7	6.7
64							3.8	4.4	4.7	5.0	5.0	5.2
80								3.0	3.4	3.7	3.8	4.0
100									2.5	2.8	2.8	3.0
125										1.9	2.0	2.2
128										1.7	1.9	2.2
160												1.5

Table 4-5. Hypergeometric Sampling Plans for Lot Sizes of 200 or Less (Acceptance Number = 2)

Sampling Size	Lot Size											
	10	20	30	40	50	60	80	100	120	150	160	200
	LTPD at 10 percent Acceptance Probability for Two Failures											
4	82	83	84	85	85	85	85	86	86	86	86	86
5	69	73	74	74	74	75	75	75	75	75	75	75
8	42	49	49	52	52	52	53	53	53	53	53	53
10		39	42	42	43	43	43	44	44	44	44	44
16		22	25	27	27	27	28	29	29	29	29	30
20			19	21	22	22	23	23	23	23	24	24
25			13	16	17	17	18	18	18	18	19	19
32				11	12	13	14	14	14	14.5	15	15
40					8.9	9.8	11	12	12	12	12	12
50						6.9	8.1	8.4	8.6	9.0	9.3	9.5
64							5.7	6.2	6.6	7.1	7.1	7.4
80								4.5	4.9	5.4	5.4	5.6
100									3.5	3.9	4.0	4.4
125										2.8	2.9	3.3
128										2.6	2.9	3.2
160												2.3

A lot of 80 semiconductor networks requires that a particular inspection satisfy acceptance to an LTPD of 5 percent. This can be achieved by the following plan:

- Sample size—40; acceptance number 0 (Table 4-3).
- Sample size—64; acceptance number 1 (Table 4-4).

Note that it is not possible to demonstrate the LTPD of 5 percent with an acceptance number greater than 1 since more networks would be required than are in the lot.

For the preceding example, Table 4-2 might also have been used, with the following resultant plan:

- Sample size—45; acceptance number 0. This results in an actual LTPD of approximately 3.5 percent, versus the table value of 5 percent.
- Sample size—77; acceptance number 1. This results in an actual LTPD of approximately 3.7 percent, versus the table value of 5 percent.

B. RELIABILITY CONCEPTS

1. General

Reliability of a product may be defined as the probability that the product will perform satisfactorily under specified conditions for a given period of time. The reliability of a product is a statistically derived figure of merit that is dependent upon the governing factors of performance, conditions and time duration. Each of these factors must be defined and understood because of its

influence on the final reliability figure; their definitions follow:

- "Performance" involves failure identification and consists of the amount of allowable device degradation and the characteristic tests performed to defined end point failure criteria.
- "Conditions" involve description of the environments the system offers to the product, such as ambient temperature, circuit configuration, and applied stresses.
- "Time Duration" involves specifying the length of time to be used in establishing the reliability figure, and the frequency of observation for the purpose of failure identification.

When the forementioned factors have been established, one is then able to proceed with the task of determining a best estimate of the reliability level for a given product. Data for making such estimates is obtained by observing the frequency of time-to-failure of a number of items placed on controlled tests. If the incidence of failure is studied with respect to time, then various failure distributions result. Several types of distributions will now be described.

2. Statistical Distributions

For a given population of items of like design and structure, the individual elements within the population will exhibit certain characteristics that follow an identifiable and similar pattern. In general, this pattern can be fitted to some mathematical model or distribution. Hence, when it is said that an item has an exponential failure distribution, what is meant is that its failure phenomenon or pattern conforms to, or is described by, the exponential distribution function.

3. Exponential Distribution

a. General

The exponential distribution has come to be the most widely used and accepted distribution for describing the mean life and failure characteristics of electronic components. Two of the main reasons for its popularity are: 1) it provides a good fit to observed system life test data, and 2) it is a relatively simple distribution with which to work. The exponential distribution is defined as follows:

$$f(t) = \frac{t}{\theta} \cdot e^{-\frac{t}{\theta}} \qquad (1)$$

where

for $t, \theta > 0$

t = time

θ = mean time between failures (MTBF)

$$f(t) = 0 \quad \text{elsewhere.} \tag{2}$$

The cumulative distribution function is given by:

$$F(t) = \int_0^t \frac{1}{\theta} \cdot e^{-\frac{t}{\theta}} \, dt \tag{3}$$

Therefore F(t) is defined as the definite probability of failure with respect to time.

$$F(t) = 1 - e^{-\frac{t}{\theta}} \tag{4}$$

The probability of success for any operation, is defined as one (1) minus the probability of failure. Therefore reliability is derived from F(t) as follows:

$$R(t) = 1 - F(t) \tag{5}$$

$$R(t) = e^{-\frac{t}{\theta}} \tag{6}$$

and finally, the failure rate (at any given point in the life) of the device is given by:

$$\lambda = \frac{f(t)}{R(t)} \tag{7}$$

$$\lambda = \frac{1}{\theta} \tag{8}$$

It is customary to assign a confidence level to reliability estimates. To state a failure rate (λ) at a given confidence level, one should use the χ^2 (chi square) distributions in the following manner:

$$\lambda \leqslant \frac{\chi^2 \alpha, (2r + 2)}{2T} \tag{9}$$

where

r = the number of observed failures

T = nt = total test hours

n = sample size

t = time required for test

Alpha (α) is found by setting the desired confidence level (C_L, in percent) equal to $(1 - \alpha)$ 100 percent, or:

$$C_L = (1 - \alpha)\ 100 \text{ percent} \tag{10}$$

The upper confidence limit* (UCL) is the most useful limit, and since it represents the most pessimistic view, the discussion will be limited to the UCL.

b. Sample Computation of Failure Rate

A sample computation of failure rate, based on the upper confidence limit, will be presented here. Assume that 1000 devices were placed on test for 2000 hours, and that one unit failed after 1000 hours of operation. To calculate the failure rate (λ) at 90 percent UCL, proceed as follows:

- Evaluate "T," the total test time:

$$T = nt$$

$$T = (999 \cdot 2000) + (1 \cdot 1000) \tag{10a}$$

$$T = 1{,}999{,}000$$

$$T \approx 2 \cdot 10^6 \text{ hours}$$

- Determine "r," the number of observed failures:

$$r = 1 \tag{10b}$$

- Determine degree of freedom:

$$2r + 2 = 4 \tag{10c}$$

- Evaluate "α";

$$\begin{aligned} (\text{UCL}) &= (1 - \alpha)\ 100\% \\ 90\% &= (1 - \alpha)\ 100\% \\ \alpha &= 0.1 \end{aligned} \tag{10d}$$

- The failure rate "λ" is computed by substituting into Equation (9).

$$\therefore \lambda \leqslant \frac{\chi^2\,(0.1,4)}{2T} \tag{11}$$

The expression for χ^2 indicates that the probability is 0.1 that a sample with four (4) degrees of freedom, taken from a normal distribution, would have $\chi^2 = 7.77$ or larger.**

$$\lambda \leqslant \frac{7.77}{4 \times 10^6} \tag{11a}$$

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* Igor Bazovsky, *Reliability Theory and Practice*, (Englewood Cliffs: Prentice-Hall, Inc., 1961), Chap. 22.

** The value of χ^2 may be found by referring to a handbook of statistical tables.

$$\lambda \leqslant 1.9 \cdot 10^{-6}$$
$$\lambda \leqslant 0.19 \cdot 10^{-5} \qquad (11b)$$
$$\lambda \leqslant 0.19\%/1000 \text{ hours}$$

c. Additional Methods for Expressing Failure Rate

General. In the previous example, the final extimate was expressed in percent per 1000 hours. This is one of several methods of expression currently in use today. Two other popular methods of expressing failure rates are: failures per hour, and failures per 10^6 hours. "Failures per hour" is very seldom used for electronic components with low failure rates because it necessitates the use of unweildy notations. (For example, the previously calculated failure rate (0.19%/1000 hours) would have to be written as 0.0000019 failures per hour.)

"Failures per 10^6 hours" is the method most often employed by systems reliability engineers in plotting failure rate charts (Figures 4-3 through 4-8). This method makes for ease in calculating a system MTBF, which is made up of a combination of all the component MTBF's. The popularity of "percent per 1000 hours" lies in the fact that it is expressed in every day terminology that is easily understood, and it is widely used in the semiconductor industry as well as in MIL-STD publications.

How to Use Failure Rate Charts. The failure rate charts shown in Figures 4-3 through 4-8 have been computed for the 90-percent and 60-percent upper and lower confidence levels, assuming 0, 1, 2, 3, 4 and 5 failures respectively where the distribution of failures is exponential. The charts are provided as a handy reference for finding failure rates without going through the lengthy calculations presented previously. To use the charts, one has only to compute total test hours (T = nt), locate nt on the horizontal axis, and find the intersection of nt and the desired confidence level; the desired failure rate can then be found on the vertical axis. The sample computation presented in Section II-B-3b, is marked on Figure 4-4 for reference.

4. The Weibull Distribution

a. General

The most recent distribution to be introduced into reliability work is the Weibull distribution. It came about as the result of failure experiences on recent technology in electronic devices which could not be fitted to any known distribution. The Weibull distribution includes three parameters: α, β, and γ. The alpha and beta parameters determine the scale and shape of the distribution; the gamma parameter is termed the location parameter and is associated with reliability work, it is generally assumed that a particular item is subjected to failure from the instant it is put on test; hence, it may be assumed that $\gamma = 0$. With this assumption in mind, the Weibull distribution function is defined as:

$$f(t) = \frac{\beta(t^{\beta} - 1)}{\alpha} \cdot e^{-\frac{t^{\beta}}{\alpha}} \qquad (12)$$

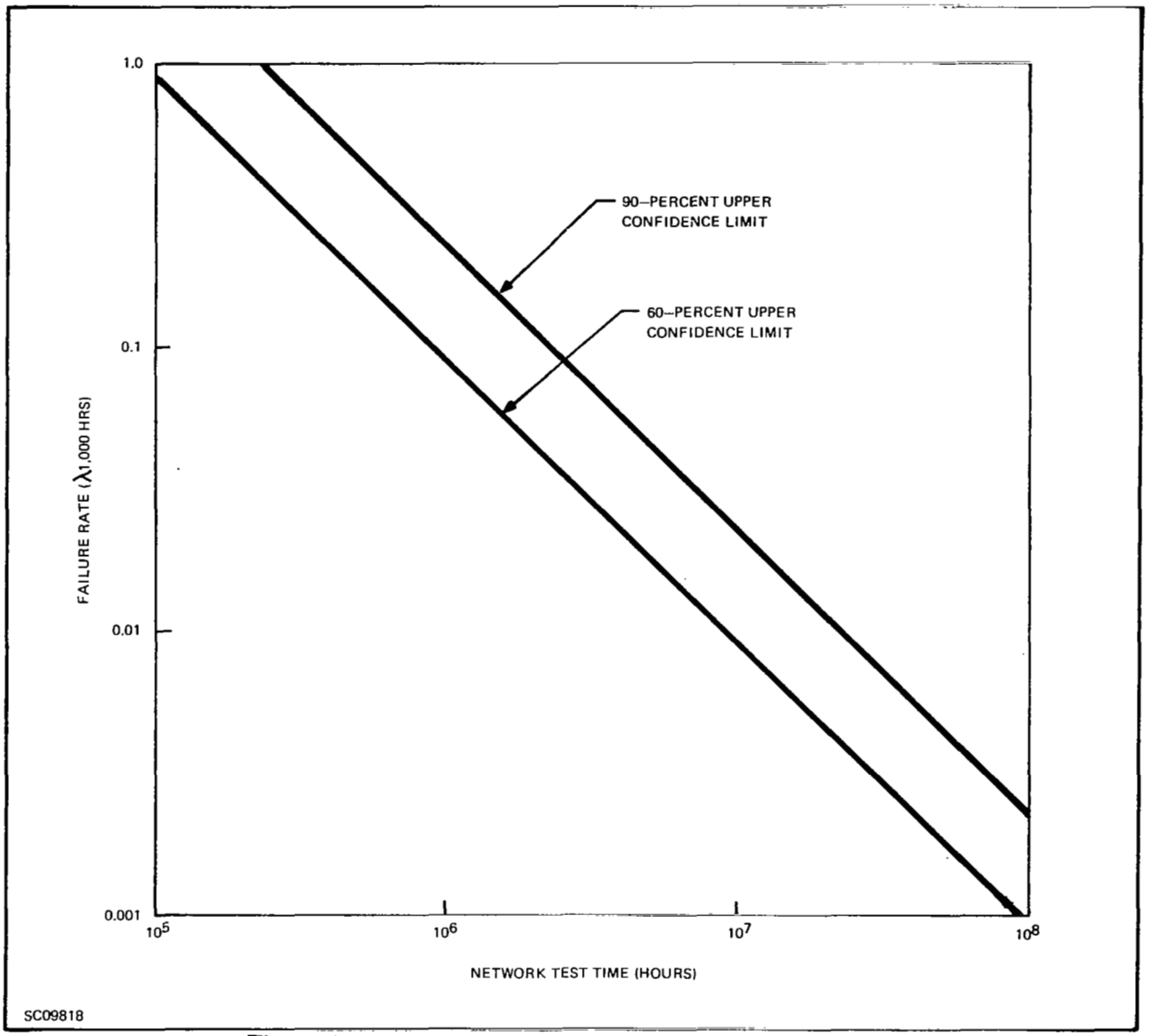

Figure 4-3. Upper Confidence Limits for Zero Failures

where

$$\text{for } \alpha, \beta, t > 0 \qquad f(t) = 0 \tag{13}$$

elsewhere.

It is evident that when $\beta = 1$ the above distribution reduces to the exponential, where alpha then becomes theta; this is illustrated in Figure 4-9(a). If β is equal to three or more, the curve begins to approach the normal or Gaussian distribution (to be discussed later), as is shown in Figure 4-9(c). For β less than one the curve resembles the exponential but with a much steeper drop-off, as is

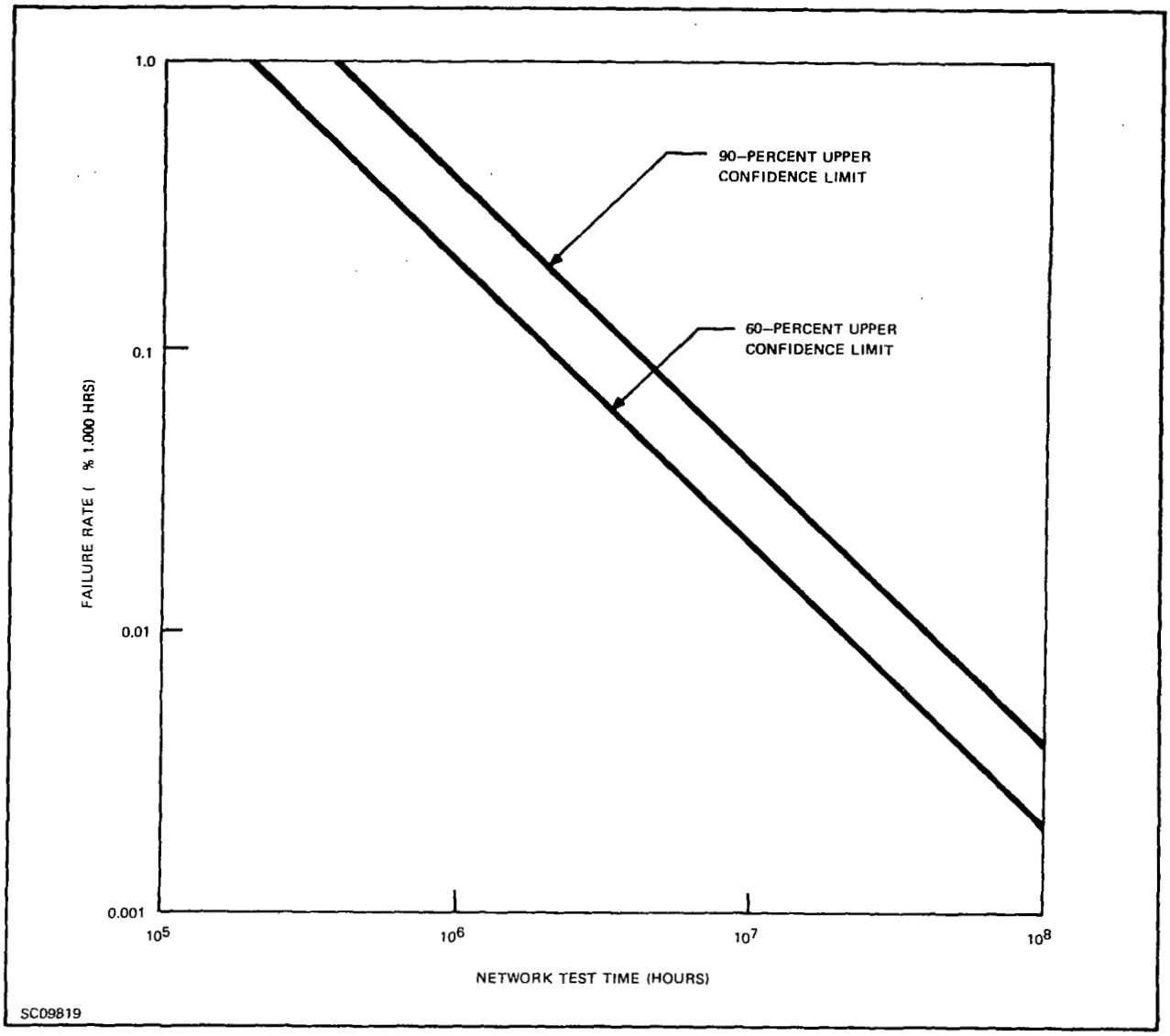

Figure 4-4. Upper Confidence Limits for One Failure

shown in Figure 4-9(e). The instantaneous failure rate (hazard rate) at time t is given by:

$$h(t) = \frac{\beta(t^{\beta} - 1)}{\alpha} \qquad (14)$$

for $\alpha, \beta, > 0$

When dealing with failure rates, the Weibull shape parameter, β, is of significance because it describes the rate of decrease (or increase) of the failure rate. The associated failure rate curves for β = 1, 3, and 0.5 are shown in Figure 4-9(b), 4-9(d), and 4-9(f), respectively. When $\beta>1$ the failure rate is an increasing function of time; when β = 1 there is a constant (exponential) failure rate with

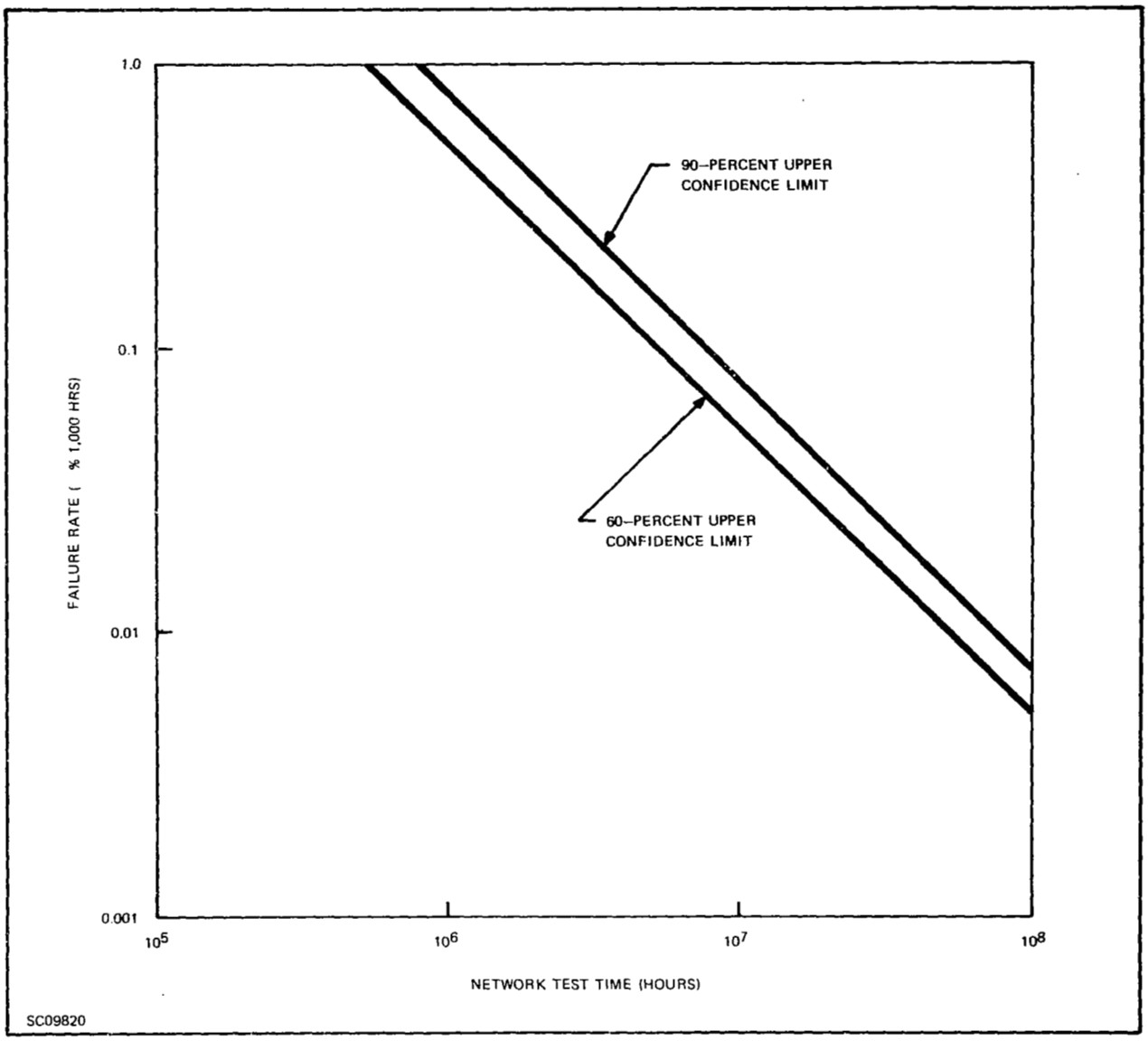

Figure 4-5. Upper Confidence Limits for Two Failures

time; when $\beta<1$ there is a decreasing failure rate with time. Although the Weibull distribution comes closer to giving a true representation of the life characteristics of semiconductor devices, it has not, as yet, been too widely accepted by the industry. The exponential distribution is still the most commonly accepted one in computing reliabiility levels. One of the primary reasons for this is the difficulty one encounters when attempting to determine the parameters α and β. A brief discussion of how to apply the Weibull distribution will now be presented.

b. Application of The Weibull Distribution

General. This discussion is based on the use of Weibull probability paper. Taking the double logarithm of the Weibull cumulative density function yields:

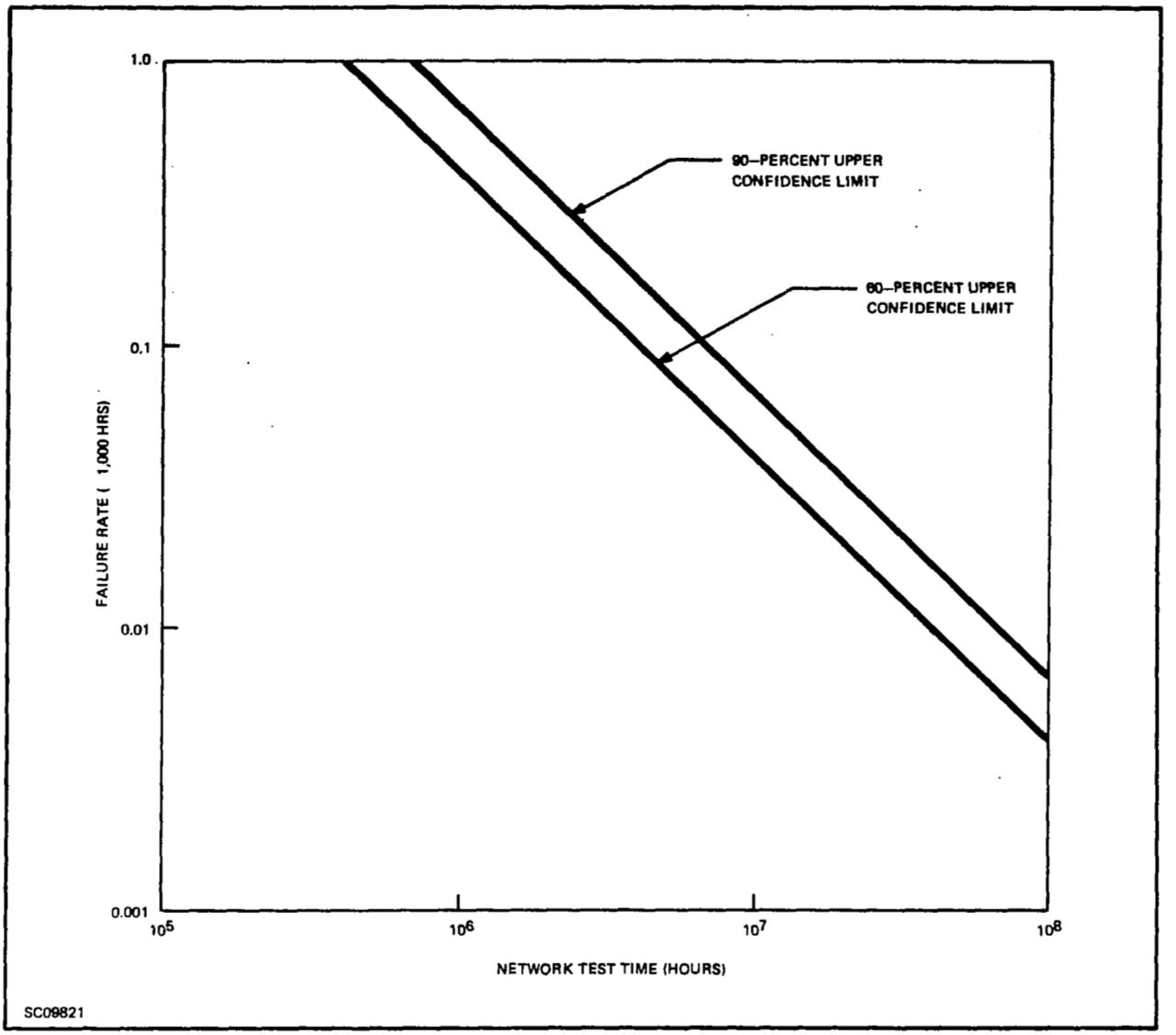

Figure 4-6. Upper Confidence Limits for Three Failures

$$\ell n \ \ell n \ \frac{1}{1 - F(t)} = -\ell n \ \alpha + \beta \cdot \ell n \ t \qquad (15)$$

which will plot as a straight line on graph paper with a $\ell n - \ell n$ versus ℓn coordinate system. The Weibull probability paper is shown in Figure 4-10. This type of graph paper has four scales. The upper and right hand scales are the Weibull scales and are linear. The lower and left hand scales are nonlinear auxiliary scales that are used to facilitate the plotting of raw data. A sample computation will be presented next to demonstrate the use of the Weibull paper.

Sample Computation of Failure Rate, Illustrating Use of Weibull Probability Paper

General. To illustrate the use of Weibull probability paper, a sample computation of the failure rate with respect to time (hazard rate) will be presented here. Assume that a sample of size n = 100

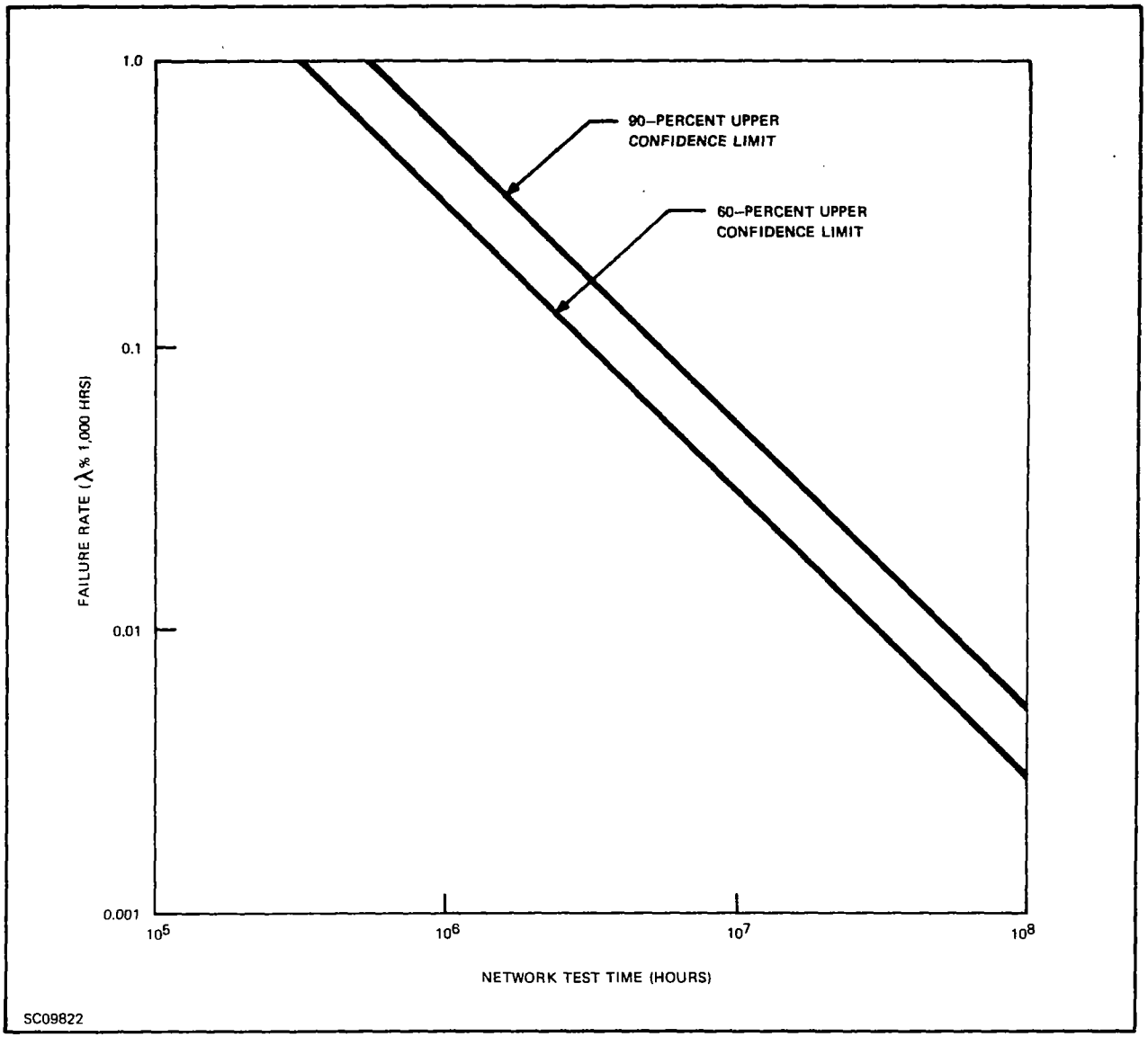

Figure 4-7. Upper Confidence Limits for Four Failures

was placed on test for 2000 hours, with reading intervals at 500, 1000, 1500, and 2000 hours. Three failures occurred at 500 hours, two at 1000 hours and one each at 1500 and 2000 hours. Distribution data for this sample problem is presented in Table 4-6.

The failure rate is computed in the following manner:

- Plot cumulative percent failed versus class mark, using the lower and scales. (See Figure 4-10.)
- Draw a "best fit" straight-line through the data points.
- The parameters α and β may now be determined. β is given by the slope of line drawn through the data points. For this example it is:

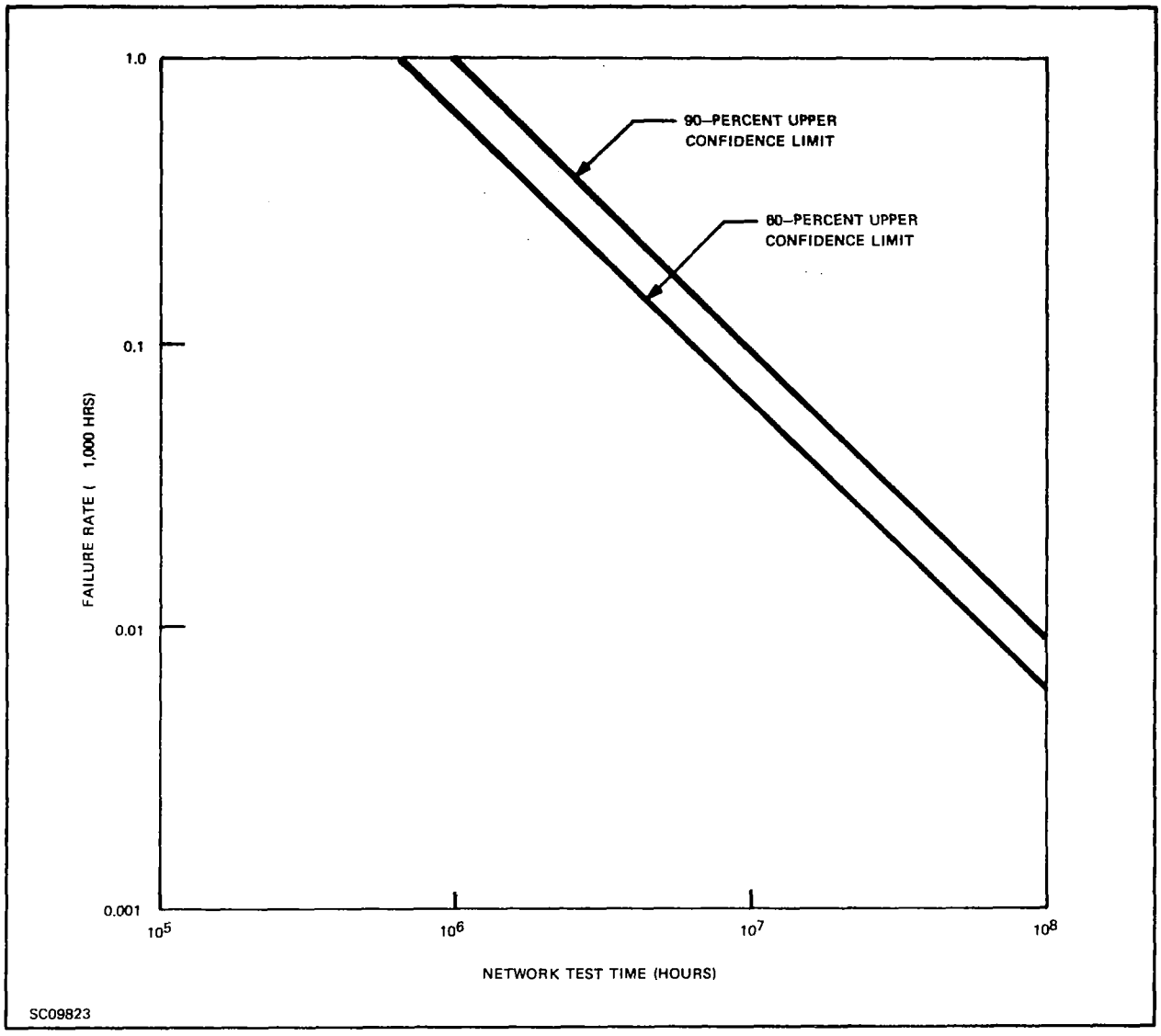

Figure 4-8. Upper Confidence Limits for Five Failures

$$\beta = \frac{\Delta y}{\Delta x} = \frac{3.9 - 1.8}{4.6} = \frac{2.1}{4.6} = 0.46 \qquad (16)$$

where

Δy is determined from the right-hand scale
Δx is determined from the upper scale

- $-\ell n\ a$ is given by the y intercept, in this case, -3.9; hence $\ell n\ a = 49.4$. Note, however, that the failureage (lower) scale was altered by the factor 10^2 in order to accommodate the data plots. By this procedure, effectively, a linear transformation on the Weibull distribution has been performed by letting $x = ct$, hence the preceding estimate for a must be multiplied by the appropriate factor to compensate for the transformed scale. Substituting $t = x/c$ in the cumulative density function,

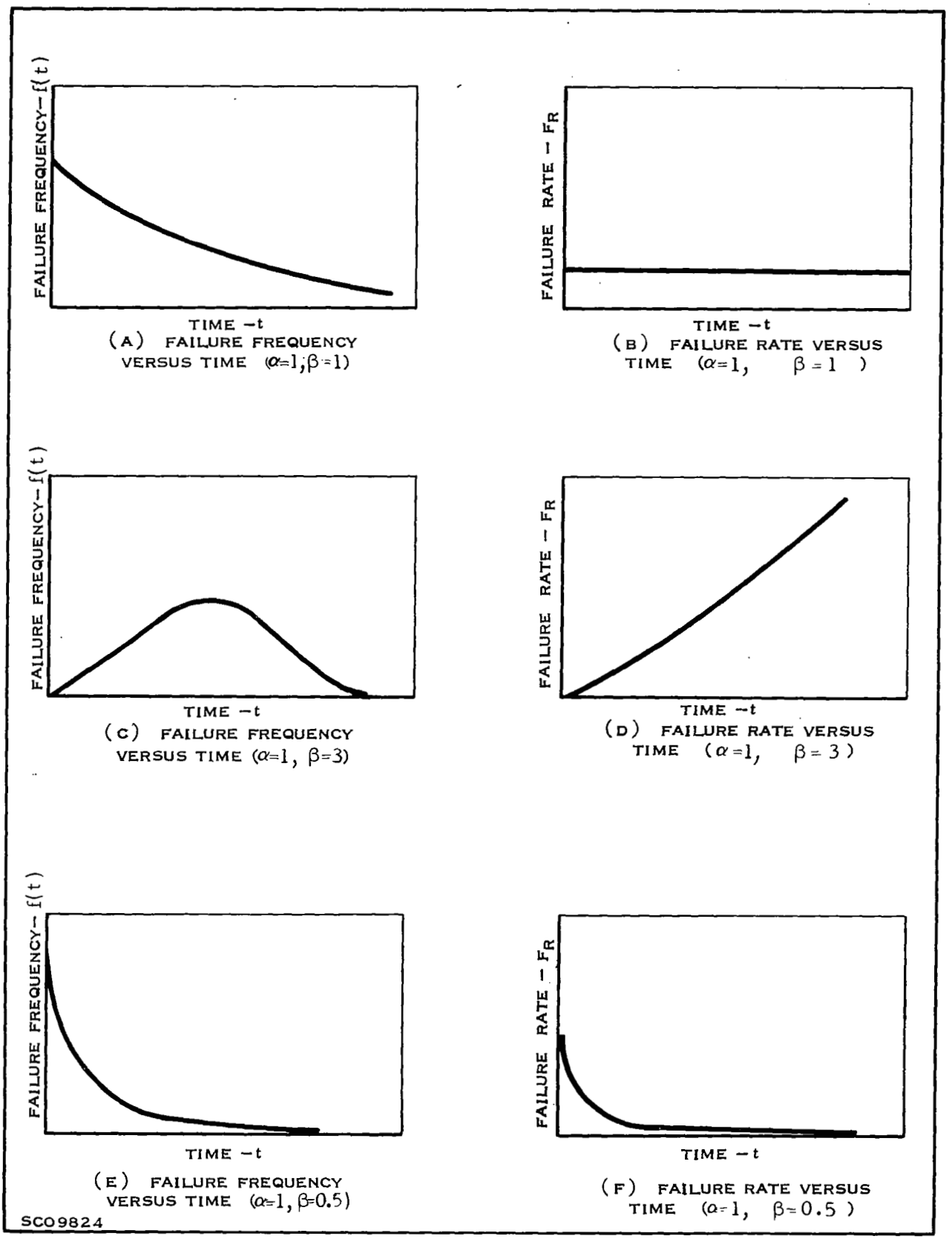

Figure 4-9. Weibull Distributions

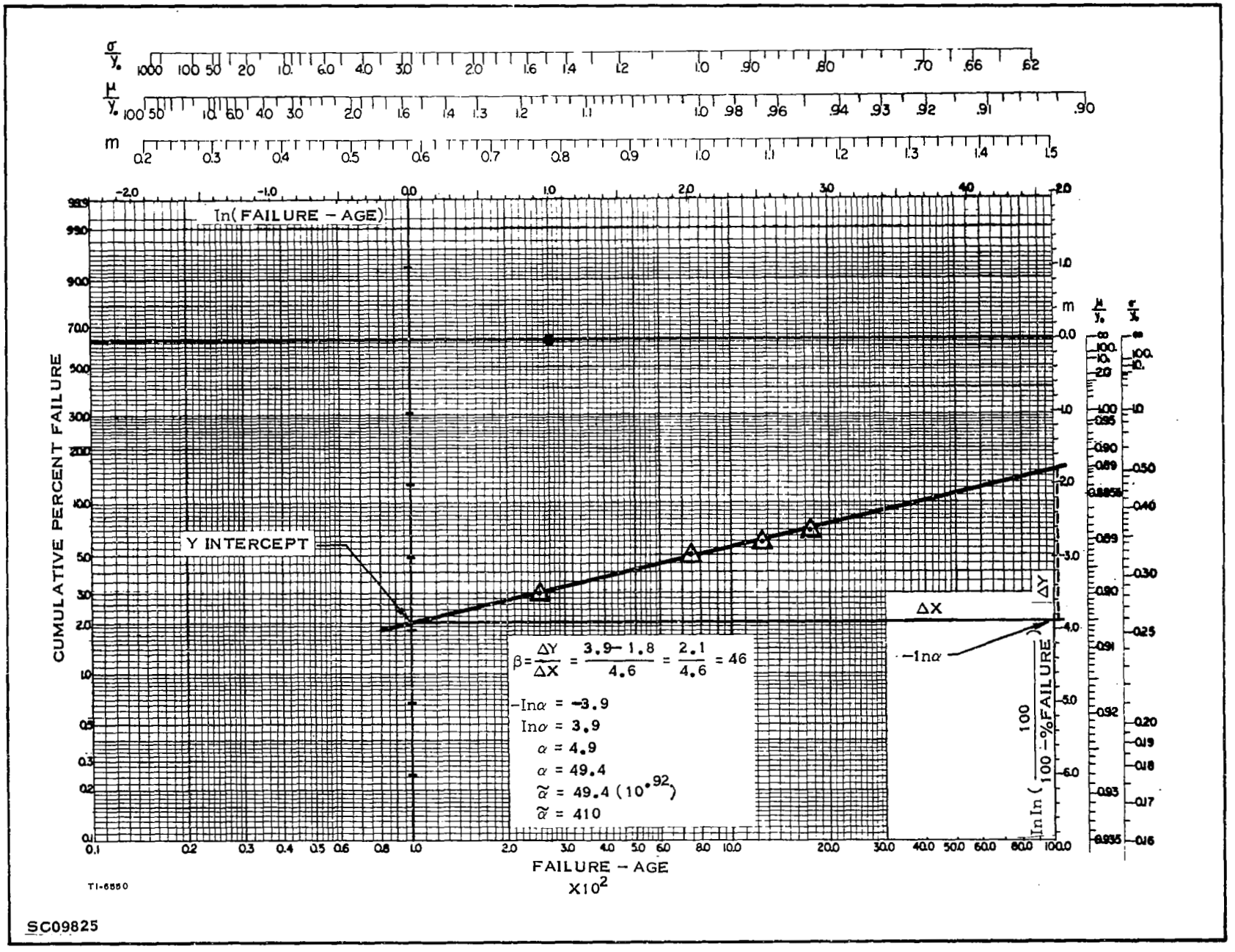

Figure 4-10. Weibull Probability Plot for Determining α and β

the scale factor for a is found to be $10^{2\beta}$, or in general, $10^{k\beta}$ for any given 10^{k} transformation. The true alpha now becomes $49.4(10)^{0.92}$ or 410.

- With a and β determined, one is now able to calculate the failure rate with respect to time (Hazard Rate) by merely substituting a desired value of t into the relation:

$$h(t) = \frac{\beta (t^{\beta} - 1)}{\alpha} \qquad (17)$$

Table 4-6. Weibull Distribution Data For Sample Problem

Test-Time Readings (hour)	Interval (hour)	Class Mark (hour)	Failures	Cumulative Percent Failed
0	-	-	-	-
500	0-500	250	3	3
1000	500-1000	750	2	5
1500	1000-1500	1250	1	6
2000	1500-2000	1750	1	7

As was stated earlier (and as will be shown in Section IV), normal life testing of monolithic microcircuits cannot generate a sufficient number of failures with which to estimate the a and β parameters. However, a sufficient amount of "burn-in" (a high reliability screening technique wherein units are operated at maximum voltage and temperature limits) has been conducted with which to make accurate failure rate curves for the early life (i.e., $t<500$ hours) characteristic of monolithic microcircuits. Several failure-rates versus time-plots that were generated on recent burn-in data are shown in Figure 4-11. The graphs show clearly that burn-in times of between 100 and 300 hours are sufficient for eliminating a majority of the early life failures (infant mortality). The monolithic microcircuit industry has tended toward using 168 hours (i.e., one week) as the recommended burn-in period. This has been done for two reasons:

- A one-week burn-in greatly simplifies logistics problems associated with processing units.
- After approximately 240 hours of burn-in, the rate of decrease in the failure rate is such that further gains in reliability are offset by additional costs of burning-in the units.

5. The Normal (Gaussian) Distribution

Unlike the exponential and Weibull distributions that deal mainly with life and failure patterns, the normal distribution is most commonly used to describe the characteristic patterns of measurable attributes. For example, if one chooses to measure the logical "zero" output voltage level of a sample of DTL gates drawn from the same lot, one would expect the readings to lie in the

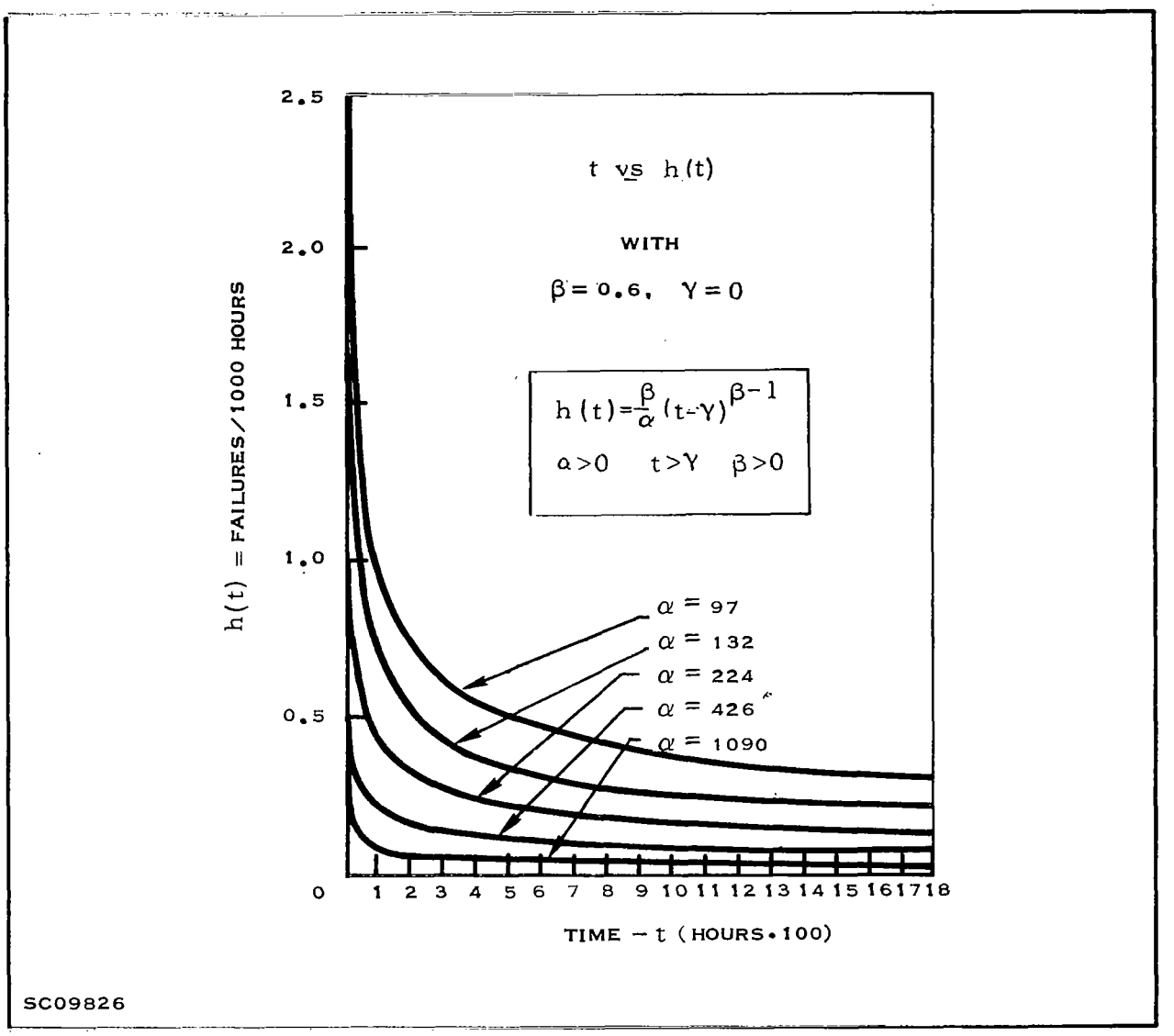

Figure 4-11. Hazard Rate (Instantaneous Failure Rate)

same neighborhood, that is, to have a central tendency. When a sample of measurements displays this characteristic, it is said to be "normally distributed."

A computer listing for a set of logical "zero" output voltage readings that has a normal distribution is shown in Figure 4-12. The normal distribution is defined as:

$$f(x) = \frac{1}{\sigma\sqrt{2\pi}} \cdot e^{-\frac{(x-\mu)^2}{2\cdot\sigma^2}} \qquad (18)$$

FREQUENCY DISTRIBUTION REPORT

DEVICE SN7370 CARD 1 DATE CODE LOT NO. S-0210 DATE READ 08-22-66 TIME INITIAL JOB SET

THIS DISTRIBUTION CONTAINS READINGS OF ONLY PASSING UNITS ON THIS PARAMETER

PAR 2 ON VOLTAGE TEST PIN 14 MIN MAX 0.30 UNIT V

GREATER THAN	LESS THAN OR EQUAL TO	PERCENT PER CELL 10 20 30 40 50 60 70 80 90 100	PERCENT PER CELL	CUM PERCENT	NUMBER PER CELL
UNDER	0		.00	.00	0
.0	.0100		.00	.00	0
.0100	.0200		.00	.00	0
.0200	.0300		.00	.00	0
.0300	.0400		.00	.00	0
.0400	.0500		.00	.00	0
.0500	.0600		.00	.00	0
.0600	.0700		.00	.00	0
.0700	.0800	XXXXXXXX	8.00	8.00	2
.0800	.0900	XXXXXXXXXXXXX	12.00	20.00	3
.0900	.1000	XXXXXXXXXXXXXXXXX	16.00	36.00	4
.1000	.1100	XXXXXXXXXXXXXXXXXXXXXXXXXXXX	28.00	64.00	7
.1100	.1200	XXXXXXXXXXXXXXXX	16.00	80.00	4
.1200	.1300	XXXXXXXXXXXX	12.00	92.00	3
.1300	.1400	XXXXXXXX	8.00	100.00	2
.1400	.1500		.00	100.00	0
.1500	.1600		.00	100.00	0
.1600	.1700		.00	100.00	0
.1700	.1800		.00	100.00	0
.1800	.1900		.00	100.00	0
.1900	.2000		.00	100.00	0
.2000	.2100		.00	100.00	0
.2100	.2200		.00	100.00	0
.2200	.2300		.00	100.00	0
.2300	.2400		.00	100.00	0
.2400	.2500		.00	100.00	0
.2500	.2600		.00	100.00	0
.2600	.2700		.00	100.00	0
.2700	.2800		.00	100.00	0
.2800	.2900		.00	100.00	0
.2900	.3000		.00	100.00	0
.3000	.3100		.00	100.00	0
.3100	.3200		.00	100.00	0
.3200	.3300		.00	100.00	0
.3300	.3400		.00	100.00	0
.3400	.3500		.00	100.00	0
.3500	.3600		.00	100.00	0
.3600	.3700		.00	100.00	0
.3700	.3800		.00	100.00	0
.3800	.3900		.00	100.00	0
.3900	.4000		.00	100.00	0
OVER	.4000		.00	100.00	0

SC09827

Figure 4-12. Frequency Distribution of those Devices in a Random Sample of DTL Gates which Tested "Good" on a Measurement of the Logical "Zero" Output Voltage Parameter

For

$$-\infty < x < +\infty \tag{19}$$

The parameters μ and σ are determined by the following relationships:

$$\mu \simeq \bar{x} = \frac{1}{n} \sum_{i=1}^{n} x_i \tag{20}$$

$$\sigma \simeq \bar{s} = + \sqrt{\frac{\sum_{i=1}^{n} (\bar{x} - x_i)^2}{n - 1}} \tag{21}$$

The parameter σ is of special importance in describing a population that has a normal distribution. Sigma (σ, standard deviation) is a measure of dispersion of the population around its mean (μ). The greater the value of σ the "flatter" the resulting curve. The smaller σ is, the closer the population is clustered about the mean. This is illustrated in Figure 4-13. Another unique property of σ is that by use of the upper and lower (i.e., $\pm$) σ, 2σ, and 3σ, limits one can determine in what band or interval 68.3 percent. 94.5 percents, and 99.73 percent of the population values lie, respectively.

C. DETERMINING WHICH DATA ARE MEANINGFUL

1. General

The preceding discussion dealt with ways and means of making reliability estimates and predictions based on methods of statistical analysis. The fundamental ingredient in any analysis is data; consequently, the accuracy of an estimation is predicated upon having meaningful information with which to make the analysis. Hence, the reliability analyst must exert care in choosing which data he shall use. The considerations presented hereafter may be helpful in determining which data are meaningful.

2. Adequate Failure Criteria

Adequate failure criteria are probably the most important considerations when one is analyzing a test program. Inadequate failure criteria will render worthless what otherwise would have been a sound test routine. Similarly, failure criteria that are too restrictive will tend to generate misleading results and perhaps obscure or distort the true implications of the test data. The two most frequently used failure criteria are:

- Catastrophic failure is a failure that is of such a nature as to render the device useless for performing its intended function. This type of failure usually takes the form of an open or a short.
- Degradation failure is a failure that involves a change in some specific parameter of a device, such that while not rendering the device completely useless, would alter its overall performance in a system and thereby induce a marginal systems condition.

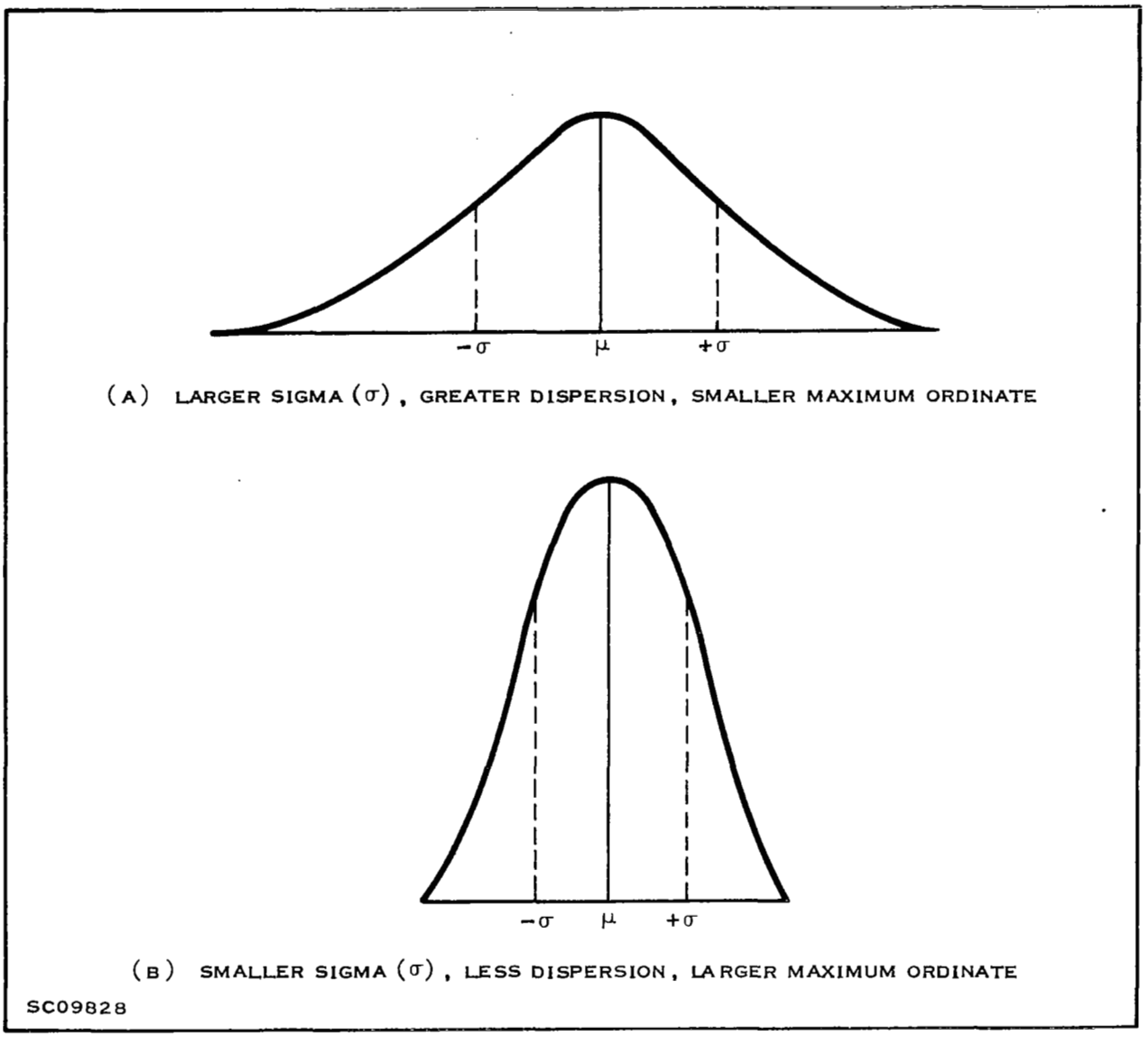

Figure 4-13. The Normal (Gaussian) Distribution

3. Contradictions in Data

All parameter test data should be carefully screened for contradictions. This question should be answered: "Do all of the failure symptoms complement each other or do they point out a possible test error?" An example of this would occur when one is testing a TTL device with multiple emitters. Suppose the data show that a particular gate failed to turn off when a trigger pulse was fed into Input No. 1 but turned "off" properly when the trigger was fed into Input No. 2. This would indicate that an open existed somewhere in the area of Input No. 1. If such were the case, some other functional test of Input No. 1 (i.e., input leakage) should also give a failure indication. If, however, all other tests involving Input No. 1 give normal readings, the test data are suspect and further verification would be necessary.

4. Errors in Test Procedure

Most errors in test procedure will manifest themselves in contradictory data, as mentioned previously. However, there are other types of errors that may escape this method of detection. Such errors in test procedure can be detected by answering the following questions:

- Was the proper ambient test temperature established and adhered to?
- Were proper voltages used (i.e., V_{cc}, V_{in}, etc.)?
- Were test technicians familiar with the test equipment and device being tested?
- Were proper failure verification procedures used?
- Were proper electrical parameters specified and tested?
- Is there adequate data traceability (i.e., person performing tests, equipment used, date, etc.)?
- Were adequate correlation procedures used, so that the data can be related to some known standard?

D. PROPER INTERPRETATION OF TEST RESULTS

Once it has been determined that the test data is accurate and meaningful, the reliability engineer is ready to interpret the test results. This is the most critical and difficult phase of making reliability predictions. The final decision will ultimately be based on a "best engineering judgement." Therefore, the following items are meant to serve only as a guideline to the interpretation of test results:

- Determine the nature and extent of any "hi-rel screen" techniques that the devices received before the evaluation was begun. (Refer to glossary of terms for a definition of "screen, hi-rel.") It is almost always true that screened devices will yield far different test results than unscreened devices. Hence, allowances should be made in order to provide compensation for any screening the sample received.
- In a well planned and executed evaluation, the engineer performing the tests should have a reasonably good idea of what he expects the test to demonstrate. Should the final results disagree with the theoretical model, a careful review of the entire program plan should be made and reasons for the disagreement established.
- The validity of the test results, and associated data generated, should be established with respect to any recent changes in the design or manufacturing processes used in fabricating the devices. This is especially true when accumulating historical data from several different sources. Using test results from a product that is no longer indicative of current production designs or methods will tend to generate misleading results and false conslustions.
- The results of the test should be compared with any historical data available. Any deviations from past trends should be noted, and reasons should be established for any changes that occurred.

SECTION III

RELIABILITY VERSUS DEVICE TYPE

A. GENERAL

The purpose of this section is to describe actual experience gained in determining failure rate by device type. While considering the steps and procedures that were followed, one should remember that all failure rates are to some extent estimates, since the inherent or true reliability can only be approached in tests or use condition estimates.

Failure rates for an operating temperature of 55° C, ranging from a low of 0.005 percent/1000 hours to a high of 0.100 percent/1000 hours, are shown in Section IV. Keeping this in mind, the easiest approach to determining device type failure rate would be simply to go to the appropriate table, select a temperature, and apply the estimated failure rate. However, an example of the fallacy of this approach is illustrated in the case of a designer who chooses to employ TTL devices. Since he has a low power application, he decides that the storage data is most pertinent. He further chooses a 25° C operating number. Consequently, he selects the failure rate, "0.038 percent/1000 hours." Note however, that in recent use-condition data on TTL parts in a large-scale digital system, some 45,000 limited temperature TTL parts have generated 224,800,000 hours of operation time with only 4 failures—a failure rate of 0.0023 percent/1000 hours, and an order of magnitude better than our imaginary designer's chosen number.

The point of this is not to exaggerate the frustration in affixing a failure rate, but to appeal to the user to consider all variables in the failure rate chosen. The remainder of this section will be an attempt to define the components of the "reliability band," which is pictorially represented in Figure 4-14. At the end of the section, there is a suggested approach to weighting the input factors of Figure 4-14 to allow assignment of system failure rates.

B. STRESS APPLIED

1. Mechanical Stress

The extremes of stress consideration are usually fairly well defined, and in general, mechanical stresses at the system level do not have as large an impact as the electrical stress. In many instances, mechanical stresses in board-assembly operation are more severe than will be encountered in system operation, and heavy consideration need not be given to mechanical environments in failure-rate determination. If high stress levels are to be experiences, such as extreme temperature cycling, or mounting shocks that can be increased by system harmonics, it would be well to consider additional component environmental stressing (screening) similar to the system environment expected and/or screening at the sub-system level.

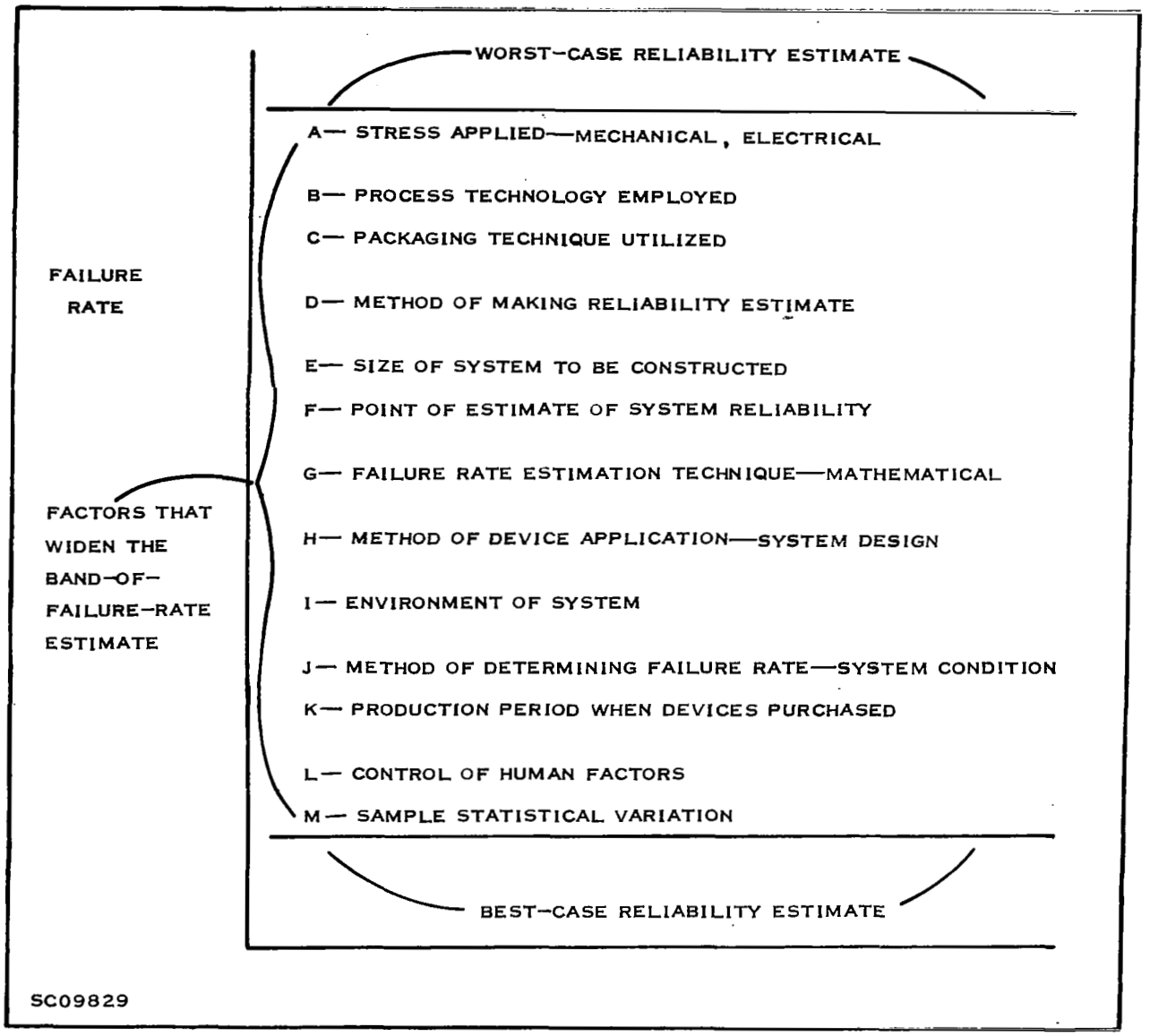

Figure 4-14. The Reliability Bandwidth

It is extremely difficult to determine "acceleration factors" for environmental mechanical stresses. For example, if "X" percent failure occurs at 1500 G, one does not necessarily have "X" percent/Y at 15 G, where Y is an acceleration factor which has not been determined. Again, the best way to approach this variable (mechanical stress) is to understand the system stresses and make sure the design capability of the individual component is far in excess of the system requirement.

2. Electrical Stress

Electrical stresses such as noise levels, transients, power supply tolerances, etc. are similar, solution-wise, to mechanical stresses. That is, the problem is one of design concepts that encompass system requirements.

With respect to some of the newer monolithic microcircuit products, it is not uncommon to see fully loaded operating conditions in the 100-200 mW region. By applying factors developed in Volume 1, "Application of Monolithic Microcircuits," it can be seen that this power may give a 20-to-40°C rise in junction temperature. This is a device-type variable and should be considered, since test data for all acceleration factors show that failure rates increase with temperature. This factor can then be anticipated in determining the actual temperature at which the failure rate estimate is needed.

C. THE EFFECT OF PROCESS TECHNOLOGY ON FAILURE RATE

It is apparent that some device technologies affect the device failure rate by giving rise to failure mechanisms which are peculiar to that technology. For example, consider a solder-seal device in which the lid melted at 270°C. If the application was such that at systems level this temperature would never occur, even in device mounting, then the possibility of a melted lid would not be a problem. However, if flow-solder mounting techniques were used which approached or exceeded this temperature, then it would be a problem. Therefore, it is necessary in determining failure rate with respect to device type, to consider such factors as:

- Does the process have good maturity and history?
- If it is a new process or product, does the technology have good engineering foundation?
- Are there no failure mechanisms peculiar to the technology employed?
- If there is a basic weakness, can component screening techniques be utilized to remove this weakness?
- Are controls implemented on the process to keep it under control? Are the controls adequate for the achievement of system control?
- If the process is fairly new, will the purchase cycle allow sufficient time for the process to mature?

The more positive the answer to each of the preceding six points, the more faith one can have in failure rates estimated for the device-type series.

D. PACKAGING TECHNIQUE AND ITS EFFECT ON FAILURE RATE

In the design stage, the choice of a package will likely be made with consideration for space restrictions, power dissipation, repair techniques, etc. The considerations of package technique when determining reliability are very similar to those of process technology. (Refer to Section III-C.) In fact, the same six points could well be evaluated from a package-technology standpoint.

Particular emphasis should be placed on understanding the ramifications of the third item—"failure mechanisms peculiar to the technology employed." For example, on early (before 1965) glass-to-metal flat packs there was a need to bond from the chip to the package leads in a manner that, due to the position of the leads, resulted in the possibility of a wire-to-chip short (Figure 4-15). Later designs have corrected this deficiency by allowing "uphill" bonding so as to

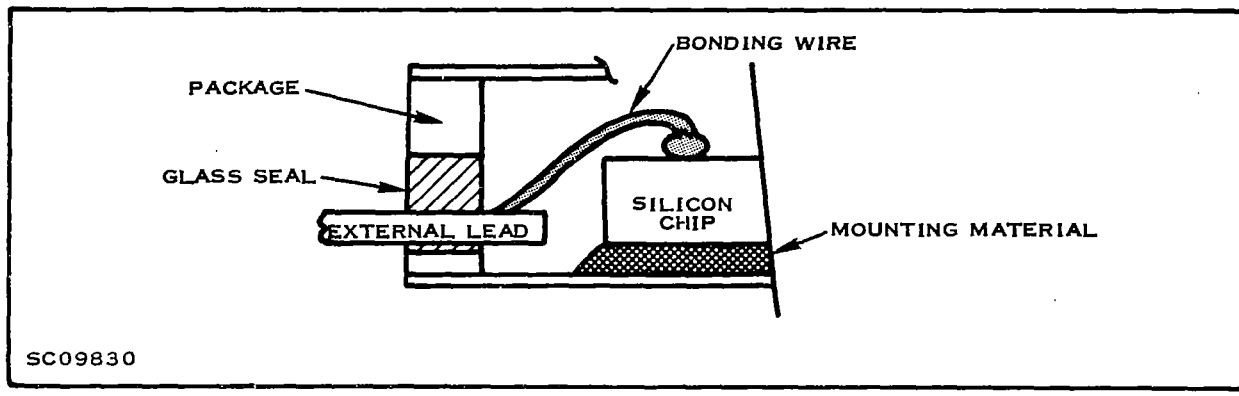

Figure 4-15. Method Used on Glass-to-Metal Flat Packs Prior to 1965 to Bond from Chip to Package Leads

preclude this possibility.* Similarly, items such as length of bonding wire runs, particularly critical internal spacing requirements, new chip mounting techniques, etc. should be considered with regard to their possible impact on package integrity.

As mentioned previously, derating factors for estimating the total effects of particular mechanisms are difficult to obtain. Engineering judgment should be used to estimate which extreme the estimated failure rate should be pushed toward—either the high or low end of the failure-rate band.

E. VARIABLES IN THE METHOD OF MAKING A RELIABILITY ESTIMATE

There are several variables in the method of making the reliability estimate. The following is a brief discussion of each of the variables that should be considered:

1) Accelerated Test Results. It is common to perform tests at higher temperatures and to derate the failure rate obtained to lower temperatures. Various derating factors are quoted by different sources. In general, the derating methods are conservative, particularly when severe stresses such as full power, full load and maximum operating temperatures are employed.

2) Use-Condition Data. Many manufacturers have access to well controlled data that is generated from large-scale, actual system operation. Provided that the system from which the data was obtained is the same as the system being designed, such data can give fairly accurate results. Part F of Section III points out some of the variables that may affect this accuracy. For example, a large-scale system of several thousand units, in a protected environment, could give different results than the use of the same component in a 100-piece system in an uncontrolled environment.

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* In this scheme, the external lead is raised above the level of the silicon chip so that the bonding wire goes "uphill" from the chip to the lead and does not approach close to the edge of the chip.

3) Reliability Processing. Accelerated data and use-condition data are commonly derived from parts which have received no special processing. User data has shown that typical reliability processing (screening) such as burn-in, temperature cycling, centrifuge, etc. give a factor-of-five improvement. Thus if a system data source gave 0.005 percent/1000 hours on standard parts, extra screening could be considered as giving a better failure rate estimate—say 0.001 percent, or it might be used to give increased confidence in the original estimate—such as 90 percent confidence versus 60 percent confidence.

Inherent in Items 1) and 2) are the possibility of human error and the extreme requirements of current failure rate verifications. Presented hereafter is an example of the extreme control over human and equipment factors that is required in a typical reliability-estimate situation.

With plenty of time available, a reliability engineer elects to run a 5000-hour life test on 2000 devices. To look at early life degradation, he elects observation times at 0, 240, 500, and 1000 hours. For complete understanding of long term performance, this engineer also observes degradation every 1000 hours thereafter, for a total of eight readings per device. He elects sixteen parameters on a fourteen-lead microcircuit as reliability indicators. The additional steps which follow illustrate the extreme control mentioned previously:

- The data storage medium (cards, tape, etc.) must read $2000 \cdot 16 \cdot 8 = 256{,}000$ readings without error. At four digits per parameters, in four bits per digit, the engineer requires 4,096,000 bits with zero errors, to prevent this error source from affecting his estimate.
- To set up loads and biases on the device, the test set might use eight relays per lead or 112 relay closures per reading or about twenty-nine million error-free closures per one life-test program.
- It will be necessary for the engineer to insert 2000 devices, eight times into the life test sockets and eight times into the test equipment sockets, and he can damage any one of fourteen leads each time he inserts a device. In other words, there will be a half-million chances for a disastrous mistake.
- Test equipment and life-test-rack transients are not to be tolerated.
- The bit error-rate in the computer that processes the data must be zero.
- And on and on—test equipment malfunction, temperature variations, mixing of serial numbers, etc.

After all of the preceding effort, if this reliability engineer has just one device failure, he will have only demonstrated a 0.02 percent/1000 hour failure rate at 60 percent UCL.

F. SIZE OF SYSTEM TO BE CONSTRUCTED

Although pure theory would not support the position, the larger-scale systems do seem to give better use-condition failure rates. This is due to the following considerations:

- In application, larger systems have a tendency to be more inaccessible for field repair. Thus, there is a smaller incidence of repair-technician error.
- The large quantities of devices make the system more insensitive to lot-by-lot device variations which could impact small systems heavily.
- Larger systems, in general, require more elaborate precautions concerning environmental exposure– or conversely, their use is such that the environment tends to be less severe–e.g., large digital computers in room ambient.

With regard to the preceding comments about a large–scale system, for a small system with a severe environment and high-reliability requirement, one might well consider a more conservative failure-rate estimate or extensive reliability screening to preclude lot variations.

G. POINT OF ESTIMATE OF SYSTEM RELIABILITY

When system reliability is being considered, it is a commonplace occurrence to measure a failure rate at several points in equipment manufacture and use. "Incoming percent defective" can be a meaningless indicator of what final system reliability will be, as it is sensitive to a manufacturer's sampling plan, his final-test electrical escape rate, his definition of failure, etc. As the system progresses through board testing and final system acceptance, the failure rate approaches more closely the inherent failure rate of the product. Considering the concept of inherent failure rate, and coordinating this with the point of estimate and the size of the system (as discussed in Section III-f), a more detailed discussion is in order.

"Inherent failure rate" is the reliability performance of a monolithic microcircuit under specified zero-tolerance conditions of power, voltage, transients, temperature, pressure, humidity, acceleration, radiation, and atmosphere, monitored and reported by an error-free data system. Observed failure rate is the more typical reliability measurement, taken at a point in time under any specific environment with its own set of operating tolerances, with observations taken by a reasonably error-free, but not perfect, man-machine combination.

The monolithic-microcircuit (or any other component) manufacturer attempts to define the inherent failure rate for his devices, since the operating tolerance of the end application environment is not under his control. How well the observed failure rate approaches the inherent failure rate depends on many hings. For instance, an orbiting satellite is a vehicle in which it is possible to approach the inherent reliability performance of a monolithic microcircuit, since the environment, even though not fully specified, follows a described, repeatable cycle. (In outer space, human intervention is not a possible cause of unintended error.)

Another meaningful example is a large system that uses many thousands of monolithic microcircuits. In this case, reliability requirements are so stringent that strict environmental control

(including human factors) is essential. Maintainability, failure reporting and failure-analysis sophistication are such that accurate microcircuit reliability data are generated. In this type of system it is possible to demonstrate the inherent reliability of monolithic microcircuits. The number of device-operating hours accumulated in a large system is so great that the perturbance of an occasional man-machine-environment error in microcircuits-failure-rate reporting can be tolerated.

In addition to providing a proving ground for microcircuit reliability, a large system can generate useful comparisons between initially observed failure rates and long-term, end-use microcircuit reliability. It has been shown that microcircuit failure rates at the system assembly, checkout, and acceptance levels will be pessimistic by an order of magnitude, with respect to microcircuit failure rates, that can be realized when the system has been finally "buttoned up" and placed in field operation.

Although the microcircuits that are manufactured for a large scale system may receive a comprehensive screening and burn-in procedure, it must be argued that the ultimate screen for these parts must remain in the end system environment. Therefore, failures generated during system assembly, check-out, and acceptance testing certainly do include escapes from the manufacturer's screening process. These can be escapes in a true-number sense from the manufacturer's procedure or can be escapes in the sense that the manufacturer's procedure does not truly represent the end system environment. Interactions with other components of the system, both electrical and mechanical, cannot be duplicated in the manufacturer's screening procedure. Also, the high-human-factors content in the reliability measurement can greatly impact the difference between observed- and inherent-failure rates.

In addition to this early system screening of unacceptable devices, it has been concluded that monolithic microcircuits demonstrate a decreasing failure rate with time. This requires that one must clearly specify the observation period for reliability verification. With a poor definition of the shape of the failure-rate distribution, one should select some resonable time period in which to make the reliability measurement. With respect to Figure 4-16, a manufacturer might assume a period between t_1 and t_2 hours when he describes inherent failure rate. Adjustments to the observed failure rate to be used by the system reliability engineer must be made of this period is not practical.

H. FAILURE RATE ESTIMATION TECHNIQUE – MATHEMATICAL

In Section I, where a more detailed discussion of mathematical considerations is presented, it is noted that the same set of raw data can give different results for the failure rate, depending on the mathematical model used. In general, even though individual component data may justify the utilization of a decreasing failure rate with time, the lower stresses of use-condition combined with a broad variety of component failure distributions give rise to system failure distributions which approach the exponential distribution function. That is, a constant failure rate with time may give satisfactory results in actual use. Certainly, if the system is predominantly semi-conductors, which characteristically have a decreasing failure rate, the constant failure rate will tend to be conservative.

Consequently, in determining failure rate by device type it is well to consider the component mix and to investigate the effects of timing (Figure 4-16) and the mathematics of the reliability estimate.

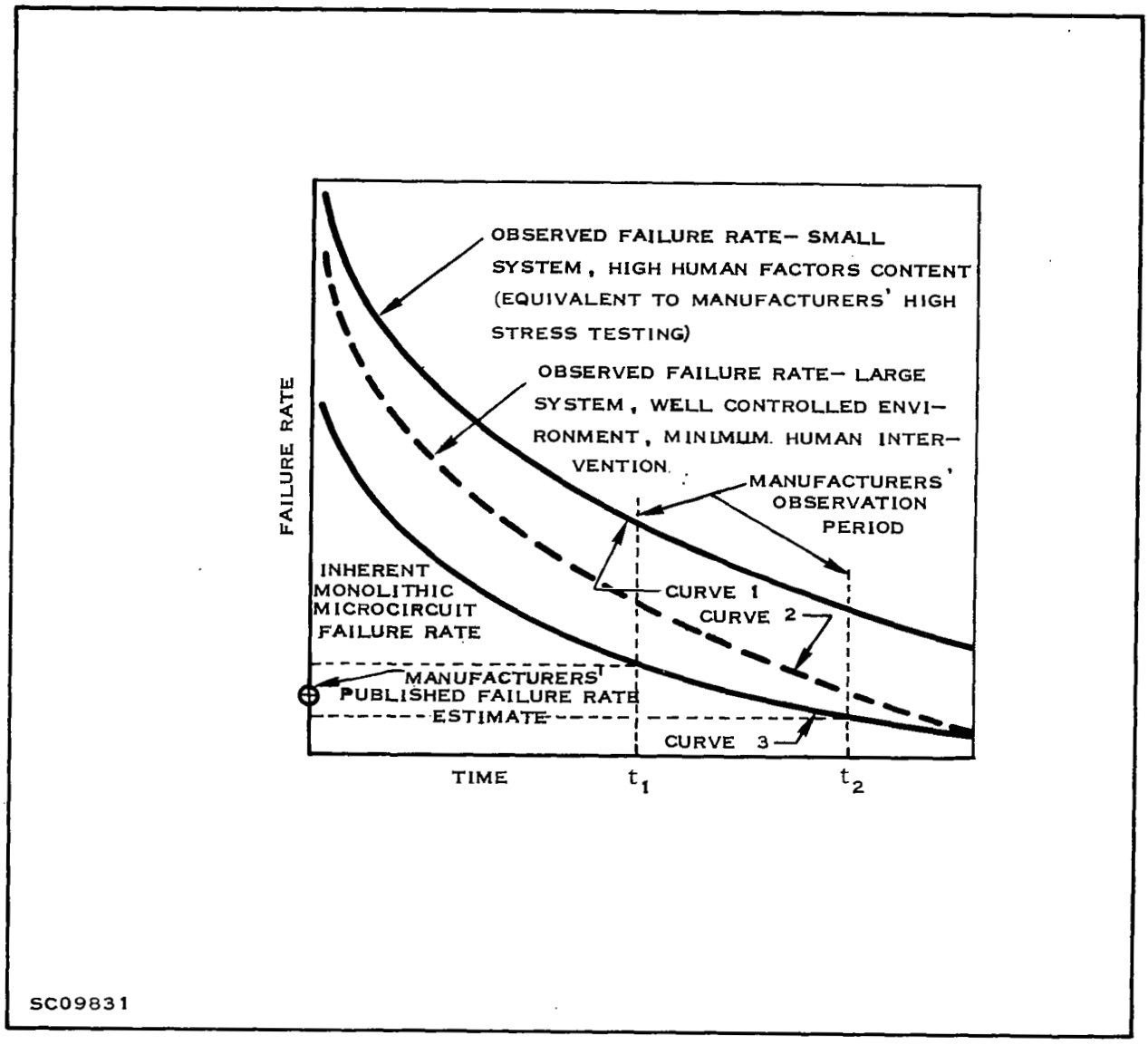

Figure 4-16. Difference Between Manufacturer's Estimate of Failure Rate and That Observed in Various Time Periods under Varying Influences of System Environment and Human Factors

I. METHOD OF DEVICE APPLICATION – SYSTEM DESIGN

In discussions with reliability engineers from systems builders, a statement of "I'm in reliability, the design stage is not my area!" brings to light a problem which can be impacted by the reliability engineer at the monolithic-microcircuit system-design stage. Many techniques which are available for making conservative designs with transistors can also be used in microcircuits. As an example, the following design practices will aid in giving a better system failure rate:

- Purchase components with electrical temperature characteristics wider than the intended system environment temperature extremes.

- Parameter guard-banding is possible to an extent but varies from device to device. Use of this technique will aid in more conservative design.
- Minimize the number of different types of circuits in the system.
- For fan-out loading, do not use maximum fan-out device capability.
- If a particularly high environmental stress is required in system application, thoroughly evaluate the capability of components to pass the stress. Use reliability processing or screening for these environments, where necessary.

All of the preceding variables can impact reliability and should be considered at the design stage. Using techniques such as these can be equally as important as considerations of device types in determining final system reliability.

J. ENVIRONMENT OF SYSTEM

The environment of the system could just as well be considered to be a design parameter in some cases. However, if it is imposed as a requirement by the system buyer, or required by the intended application, it needs to be considered as a reliability factor.

In Volume 2, "Failure Mechanisms," several failure mechanisms are discussed which are temperature dependent. Thus, a system with a 100°C maximum temperature environment (such as an avionics package) would show possibly a high failure rate than a commercial computer operating very near room ambient.

Another design factor which impacts system environment is power dissipation. Early microcircuit digital logic types, such as RTL and RCTL, commonly had low speeds and low-power dissipation. Newer ECL circuits and some linear and high-speed digital types may dissipate upwards of 100 mW of power. The operating temperatures that may be reached in a high-packaging-density system design require a thorough understanding of the effect of temperature on monolithic microcircuit reliability.

A convenient representation of the growth and current reliability estimates for typical monolithic microcircuits is shown in Figure 4-17. The vertical scale is failure rate in both failure per million hours and percent per thousand hours. The horizontal scale is the reciprocal of degrees Kelvin over 1000 (1000/°K), with most temperatures of interest indicated in degrees centigrade. Curve A shows the failure rate for standard off-the-shelf microcircuits that were evaluated in test programs conducted in 1961 and 1962. The data for this curve were collected during observations over the range of 200°C to 55°C. During the early period of monolithic microcircuits, these data were the most meaningful data available on acceleration factors. At that time there was no opportunity for estimating inherent monolithic microcircuit reliability, since no large-system history was available.

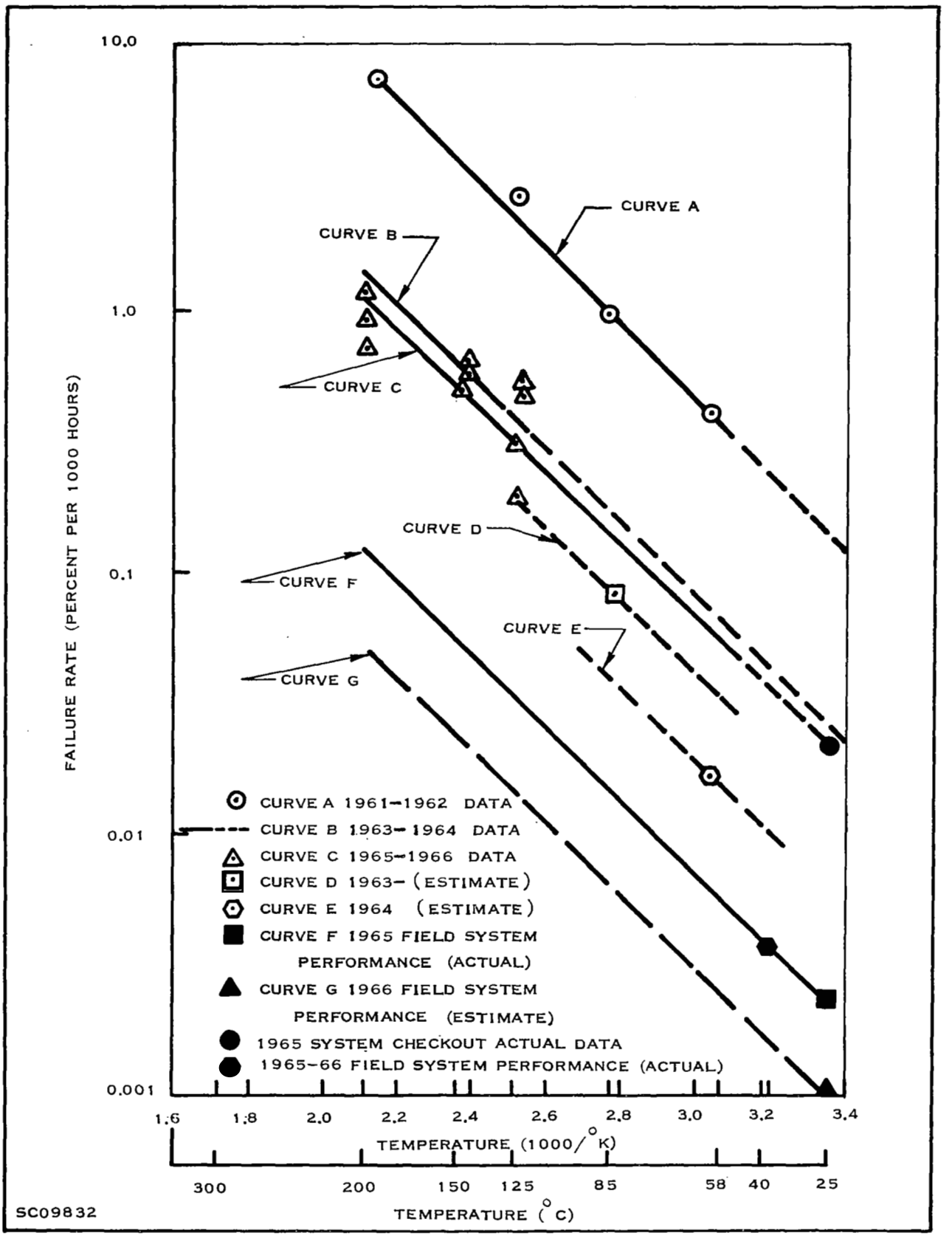

Figure 4-17. Verification of Estimated Failure Rates for Monolithic Microcircuits

Curve B is based on 1963 and 1964 data observations and shows the remarkable reliability growth of microcircuits in comparison with the 1961 and 1962 failure rate data indicated in Curve A. It should be noted that there is verification of the implication that while the failure rate of microcircuits is decreasing with time, the slope of the derating curve does not appear to change. In 1963, published estimates of microcircuit inherent reliability were in the range of 0.08 percent/1000 hours at 85°C. This estimate was based on field data being generated on early monolithic microcircuit systems. Using the same acceleration factor, one may, with moderate confidence, draw a parallel line (Curve D) through the 1963 estimate, and this curve will be the derating curve applicable to 1963 production.

By 1964, more systems data was available from field reports, and reported failure rates were around 0.016 percent/1000 hours. Now, with the same assumption of parallelism used previously, Curve E may be drawn.

In summarizing the test programs of 1965 and 1966, a number of data points were generated and are identified in Figure 4-17 as 1965-1966 data. Curve C is the "best fit" of this data. It is interesting to note that on Curve C, two of the data points relate to a large-scale field system. The first point is the 200°C storage test result. The second point is an average value of observed rate on the field system during systems buildup, checkout, and acceptance testing. The other data points are results of a manufacturer's in-house reliability assessment program on various product lines.

The closeness of Curves B and C indicate very dramatically the difficulties enumerated earlier in obtaining failure rate verification from test programs, or in fact from the preliminary stages of system assembly. It may be said that Curve C represents the manufacturer's current state-of-the-art of testing and data gathering capabilities both in high stress, worst-case reliability assessment testing and in a typical high-volume system checkout situation.

The data presently being generated by large systems in field operation present a very real point both for postulating the validity of the 1963 and 1964 estimates and for establishing an excellent representation of the inherent reliability of the 1965 production. If the derating factors are still valid, Curve F can be drawn through the 1965 field system performance data point, but if the derating factors are not valid, it is none-the-less a fact that this data point exists and is indicative of the reliability trend established for microcircuits.

Curve G (Figure 4-17) is a representation of one manufacturer's 1966 microcircuits failure rate. The curve is based on an estimate of data currently being generated in field applications. The accuracy of this estimate should be verified by the end of 1967, and it is expected to reflect the reliability growth brought about by corrective actions made to the manufacturer's products during 1966.

This discussion of system environment would not be complete without giving due recognition to "special environments" such as extreme temperature cycling, shock, acceleration, etc. Although these special environments are equally important, it is more difficult to determine appropriate acceleration factors for them. This difficulty is a consideration in the computation of failure rate, as was noted previously in Section III-1.

K. SYSTEM–CONDITION METHOD OF DETERMINING FAILURE RATE

Failure rate is affected by system condition as well as by time. In the previous discussion of the "point of estimate of system reliability" (Section III-G and Figure 4-16), it was shown that the point-in-time of part reliability can make a difference in device-failure rate. The degree of completion or checkout of the system will impact failure rate. If the system is in a use-condition environment, then the failure rate will be much lower—often an order of magnitude—than the last failure rate estimate made in the final stages of system checkout. Thus, caution should be exercised if a particularly low failure rate is to be demonstrated in final system checkout, as this failure rate may be considerably higher than the failure rate which will be experienced by the system user.

L. PRODUCTION PERIOD WHEN DEVICES PURCHASED

It is obvious that since failure rates for microcircuits improve as technology advances, the production-period origin of the devices will affect the failure rate. As the production process matures, and as more experience is gained on a particular circuit, failure rates improve. For example, published microcircuit failure rates in 1961 were about 4.0 percent/1000 hours for 55° C application. As mentioned previously, Section IV lists failure rates as low as 0.005 percent/1000 hours, or approximately three orders-of-magnitude improvement in six years.

Although it is improbable there will be a similar improvement in the next three years, continued improvement is likely. Thus, when considering the selection of a device, if one makes a decision today that is based on today's data and it is known that the devices are currently in production but will be purchased a year away, this will add confidence to the reliability estimate.

M. CONTROL OF HUMAN FACTORS

As shown in Figure 4-16, large-scale systems have better failure rates, probably due to better control over human factors. It is difficult to assess the risk of poor control over human factors. Some guides for determining the degree of risk would be items such as:

- Requirement to repair individual compoments in the field or in board checkout.
- Critical spacing requirements where individual component analysis is required.
- High-board-rework rates which render it difficult to establish standard procedures for repair work.

These guides, of course, are only types of questions which can be asked. Rigidity of checkout procedures, methods of control, etc. must all be investigated with human-factor control in mind.

N. SAMPLE STATISTICAL VARIATION

The mathematical aspects of sample variation are discussed elsewhere in the Handbook, but the concept is sufficiently important to this discussion of reliability versus device type to present some comments here.

A sample pulled from a population will be, at least, an estimate of the total population. This sample can be thought of as the one which is selected for reliability tests, or even the complete system it self, since even the largest system is only a portion of the manufacturer's output during a period of time.

O. METHOD OF APPLICATION OF RELIABILITY DATA

To make use of the information presented in this section, the following approach is suggested:

- Evaluate the system and its components, considering each of the variables in this section.
- For each variable, consider whether the application will tend to increase, decrease, or not affect the basic reliability best estimate.
- Consider whether one variable may be more critical than another, and assign a weight.
- Combine these factors for a final estimate.

An example of the application of the preceding suggestions is presented in Table 4-7.

Table 4-7. Example of Assignment of Weights to Variable Factors of Reliability Band

Effect of System Application on Variables	Variable Factors of Reliability Band (Value = "1")													Value of Weighted Variable [Σ (Application Effect) · (Weight)]
	A	B	C	D	E	F	G	H	I	J	K	L	M	
Increase	X				X		X		X		X			10
No Effect		X	X	X								X	X	5
Decrease						X		X		X				3
Weight	2	1	1	1	2	1	1	1	3	1	2	1	1	

The system presented in Table 4-7, would tend to have a higher failure rate than the best estimate would suggest. However, it should be noted that the appointment technique employed is not nearly so important as the recognition of these variables and the consideration of them in design or estimation of the final reliability estimate.

P. SUMMARY

The information in this section has been presented in response to the question, "What is the failure rate of the XXX device?" The basic objective has been to emphasize that there is no single answer to this question, and to alert the designer to some possible variables in the system and product which tend to make the estimate a band rather than a fixed number.

SECTION IV

MEAN LIFE CHARACTERISTICS

A. DISCUSSION

1. General

The mean life characteristics of monolithic microcircuits, as well as of most other electronic components, have become the most popular and widely accepted measure of reliability. Unfortunately, as was pointed out in Section II, it is the most difficult reliability estimate to obtain. This discussion contains several assumptions, all of which will be described.

2. Basic Assumptions

The basic assumptions contained in this discussion of mean life characteristics are described as follows:

- Temperature Derating. In recent years it has become apparent that the inherent failure rate of microcircuits has decreased below the 0.01 percent/1000 hours level. In order to determine a statistically significant mean life of microcircuits with such low failure rates, it is necessary to employ accelerated test techniques and to derate the end results to equivalent normal use conditions. The failure rates given in this Volume of the Handbook will be stated at three stress levels: room ambient (+25° C), a "worst-case" room ambient (+55° C), and severe environment (+85° C). The acceleration factors used to obtain these equivalent failure rates are given in Table 4-8. The derating (or acceleration) factors used in this Volume were originally determined from empirical data of test run in 1961 and 1962. The derating curve (Curve A) is shown in Figure 4-17. An accompanying curve (Curve B) plotted from data gathered in 1963-64 is also shown. The fact that the more recent curve is lower than the original curve indicates a significant reliability improvement during the associated time interval. The parallelism of the two curves shows that the same relative proportion of failures, with respect to temperature acceleration, existed at both time intervals. The fact that the slope of these two curves remained invariant over time substantiates the accuracy of the original derating factors and justifies their continued use.

Table 4-8. Temperature-Derating Acceleration Factors Used to Obtain Equivalent Failure Rates

Temperature Derating			
	To Stress Level Temperature (°C)		
To Derate From Test Temperature (°C)	25	55 Multiply Total Test Hours by Acceleration Factor	85
200°C	50	18.7	7.5
150°C	24.7	8.0	3.7
125°C	18.0	6.8	2.7
85°C	6.7	2.5	1.0
55°C	2.7	1.0	0.4
25°C	1.0	0.37	0.15

- All reliability estimates are based on an assumed exponential distribution. The underlying considerations for choosing the exponential are:
  - Life testing, even at the upper limits of device capabilities, has generated an insufficient number of failures with which to make accurate estimates of the shape and scale parameters of the Weibull distribution.
  - The exponential assumption has been firmly established and accepted by the electronics industry in that nearly all systems MTBF calculations are made from formulas that assume a constant (or exponential) failure rate for discrete electronic components.
  - The exponential assumption, in effect, takes a "worst-case" approach to stating failure rates for microcircuits, as opposed to the Weibull or Gamma distributions.
- Failure rates are stated at the 60 percent upper confidence limit (UCL).
- Failure criteria is based on the device's ability to pass selected reliability-sensitive parameters at each test interval. The number of parameter measurements made varies from 5 to 32, depending on device complexity. A listing of the parameters tested, the test conditions, and their respective limits for each device basic-logic family, are given in Table 4-9. The number and combination of the parameters tested depend upon the individual circuit type. All electrical parameter measurements conform to the following items:
  - All parameter measurements are made using worst-case input voltages.
  - All digital network measurements are performed at +125° C; linear network measurements are made at +25° C.
  - The criteria set forth here is applicable to the life, environment, overstress and parameter stability discussions in this Volume of the Handbook.

Table 4-9: Reliability-Sensitive Parameters

Monolithic Microcircuit Device (Basic Logic Family)	Parameter					Test Conditions									
	Symbol	Definition	Minimum Acceptable Value			V_{CC} (V)	V_{in} (V)	V_{out} (V)	V_1 (V)	V_2 (V)	$V_{CP(S)}$ (V)	V_R (V)	I_{load} (mA)	I_{load} (μA)	I_{sink} (mA)
			(V)	(mA)	(μA)										
RCTL	V_{off}	Logical "one" output voltage	≥ 5.0			6.0	0.3								
	V_{on}	Logical "zero" output voltage	≤ 0.3			6.0	2.0								
	I_{in}	Input current			$20.0 \leq I_{in} \leq 70.0$	6.0	2.5								
DTL (Typical gate)	V_{off}	Logical "one" output voltage	≥ 2.50			4.5	0.8						−0.12		
	V_{on}	Logical "zero" output voltage	≤ 0.45			4.5	1.7								10.8
	I_R	Logical "one" input current			≤ 5.0	5.5	4.0								
	I_F	Logical "zero" input current		≤ −1.5		5.5	0					4.0			
	I_{OS}	Short circuit output current		≤ −1.3		5.5		0							
DTL (Typical flip-flop)	V_{off}	Logical "one" output voltage at Q or $\overline{Q}$	≥ 2.50			4.5			1.7	0.8			−0.12		
	V_{on}	Logical "zero" output voltage at Q or $\overline{Q}$	≤ 0.45			4.5					0.75				9.5
	I_R	Logical "one" input current			≤ 5.0	5.5	4.0								
	I_F	Logical "zero" input current		≤ 1.0		5.5	0								
TTL	V_{off}	Logical "one" output voltage	≥ 2.40			4.5	0.8							−400.0	
	V_{on}	Logical "zero" output voltage	≤ 0.40			4.5	2.0								16.0
	I_{IL}	Input leakage current			≤ 40.0	5.5	2.4								
	I_{in}	Input current		≤ −1.6		5.5	0.4								
	I_{OS}	Short circuit output current		$20.0 \leq I_{OS} \leq 55.0$		5.5									

Monolithic Microcircuit Device (Basic Logic Family)	Parameter							
	Symbol	Definition	Minimum Acceptable Value					
			(V)	(mV)	Gain			
Linear	V_{OM}	Maximum peak-to-peak output voltage, no load	≥ 11.0			+12.0	−12.0	1.0
	V_{OM}	Maximum peak-to-peak voltage, 10 k Ω load	≥ 9.0			+12.0	−12.0	1.0
	A_V	Voltage gain			≥ 630	+12.0	−12.0	1.0
	V_{DI}	Differential input voltage offset		≤ 40.0		+12.0	−12.0	1.0

B. OPERATING LIFE

1. General

Before beginning this discussion of the mean operating life characteristics of microcircuits, a brief description of the three basic methods of conducting operating life tests will be presented.

2. Steady-State-Operating-Life Test

In the steady-state operating-life test, the circuits have a dc potential applied in such a manner as to reverse-bias or forward-bias the transistor junctions in the circuit. Typical forward- and reverse-biased circuits are shown in Figures 4-18 and 4-19, respectively. The main disadvantage of this type of testing is that digital circuits are not required to perform as they would in a system (i.e., switching "on" or "off") but rather to remain on a continuous "on" or "off" state. The steady-state mode of testing is used primarily for linear circuits.

3. Series-Switching-Life Test

The series-switching-life test circuit is commonly known as a "ring counter." This type of life test differs from the steady state in that the circuits are being toggled, (turned "on" and "off")

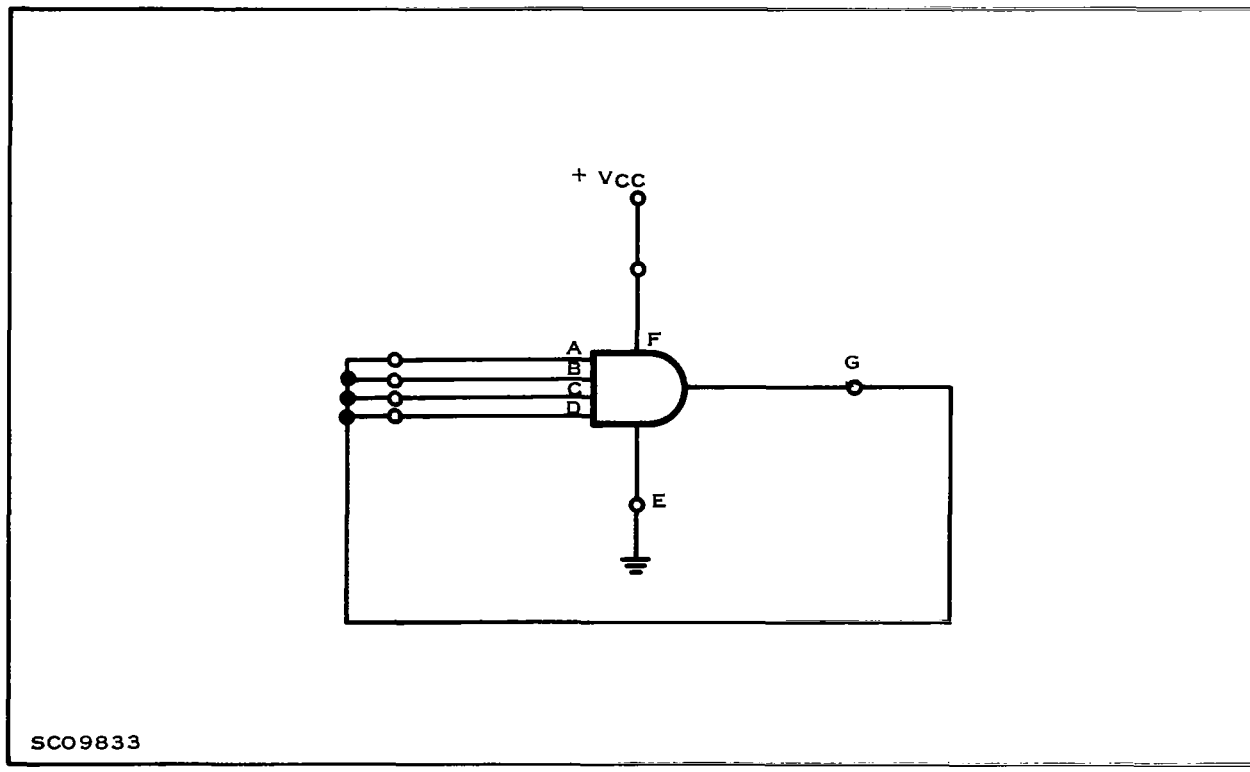

Figure 4-18. Forward Bias Test Circuit

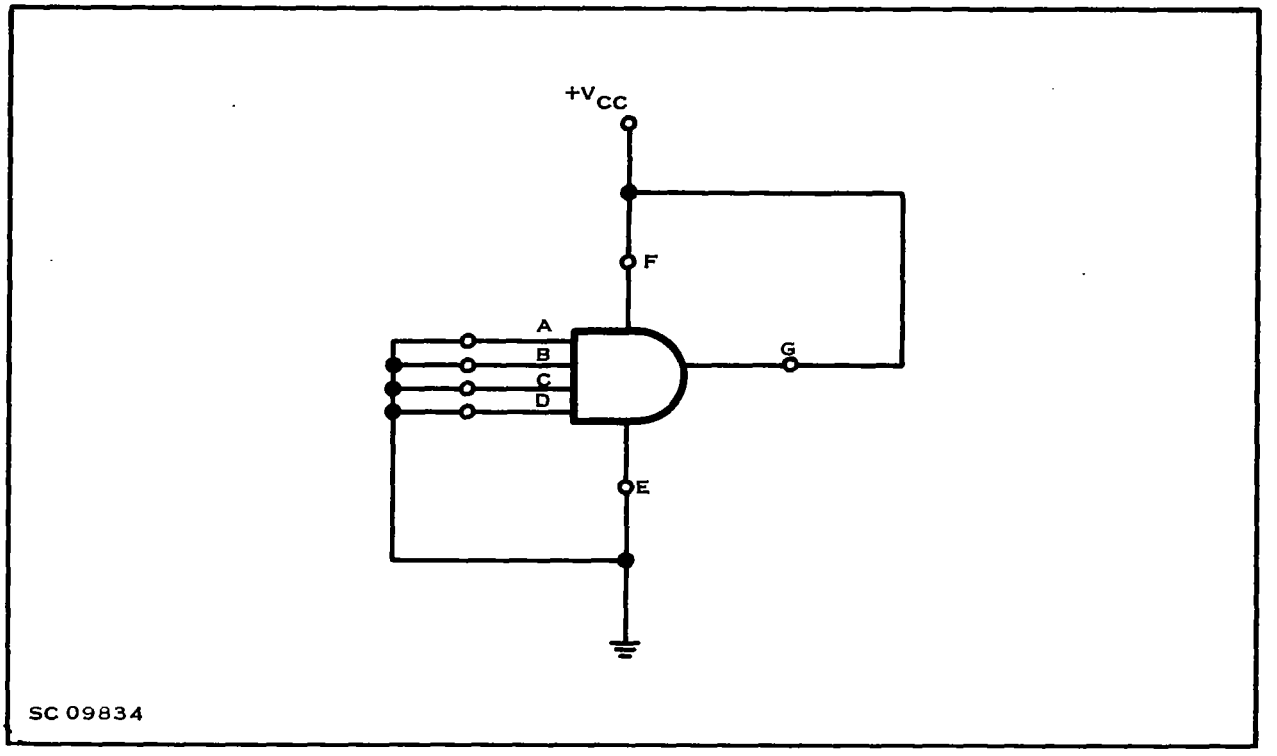

Figure 4-19. Reverse Bias Test Circuit

therefore, this test is applicable only to gates. The circuits are connected in series, with the output of one circuit driving the inputs of the following circuit. A typical ring counter is shown in Figure 4-20. The primary advantages of this type of test are that the toggling operation more nearly simulates actual in-use conditions than the steady-state test, and it is very economical to build and operate. However, the ring counter has several limitations:

- The devices are not fully loaded and are not stressed under worst-case conditions.
- The devices are not equally stressed. There are slight variations in electrical characteristics (i.e., resistors, transistor betas, etc.) from one device to another. Hence, the P_d and output loading will vary from one unit to another.
- The operation of each device in the ring is dependent upon the operation of every other device in the counter. Hence the malfunction of one unit will render inoperative the entire life-test circuit. This, in turn, necessitates much closer monitoring of the life test units, and there is an associated risk of inducing misleading results due to test errors.

4. Loaded Ringing Counter Test Circuit

The loaded ringing counter test circuit is identical to the one described previously, except that the limitation given in the first item of the preceding list if eliminated by placing a resistor in series with the output so that maximum fan-out levels may be more nearly simulated.

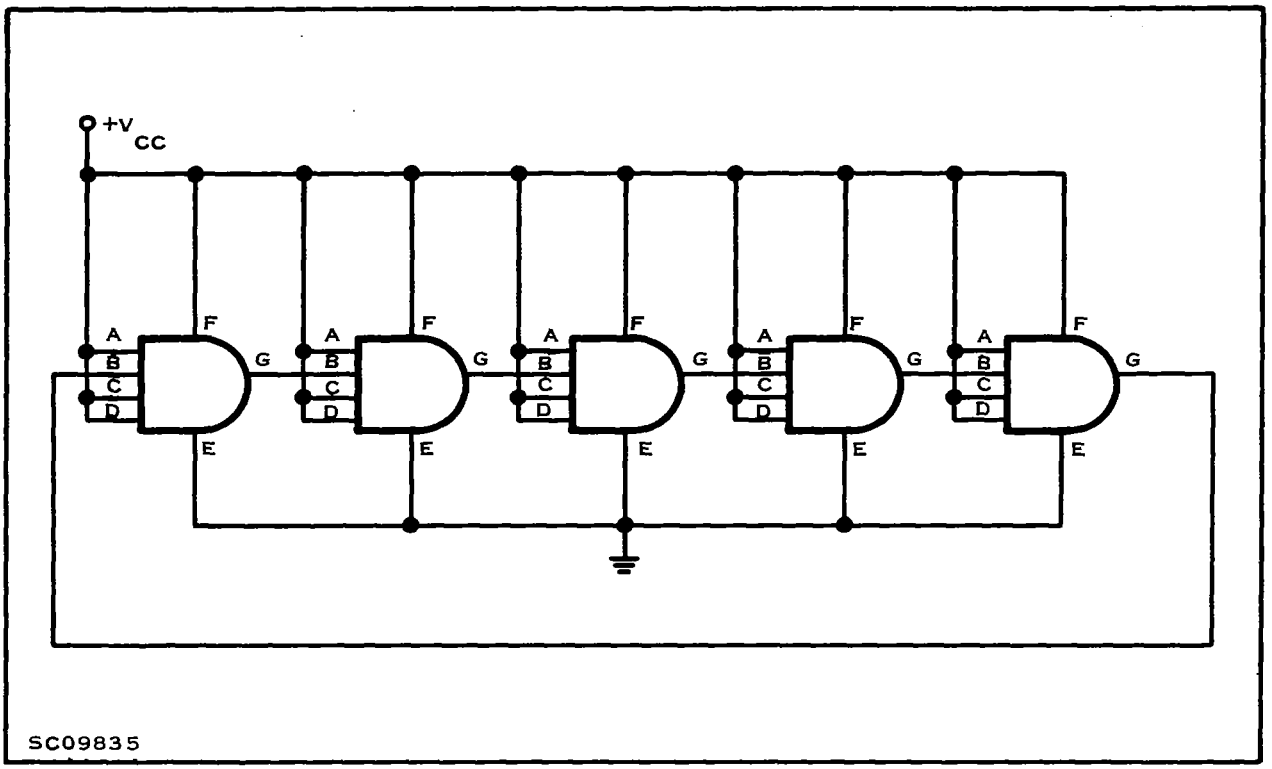

Figure 4-20. Ring Counter Test Circuit

5. Parallel-Switching-Life Test

The parallel-switching-life test circuit is similar to the series-switching-life test in that the circuits are being toggled. However, it has several advantages over the series-switching circuits:

- Each circuit is driven independently by a switching voltage, the frequency being generally 60 Hz to 100 kHz; each output is normally fed into a simulated maximum fan-out load. This insures that each and every circuit will be adequately stressed under worst-case conditions.
- Since each circuit is operated independently, a malfunction of one device will not affect the remaining devices on test.
- This type of test can be used for both digital and flip-flop circuits.
- Although this type of testing is more costly than the previously mentioned ones, it provides much more meaningful indications of worst-case circuit reliability than do the stedy-state and ring-counter tests.

6. Summary

All digital operating-life test data presented in this Handbook were generated on a parallel-switching type of life-test circuit, and the linear data were generated using a steady-state type of circuit. The mean-operating-life characteristics for each device basic-logic family presented

in Table 4-9 are summarized in Tables 4-10 through 4-13. All operating-life tests were conducted at +125°C, using worst-case input voltages. Typical life-test circuits for each generic family are given in Figures 4-21 through 4-24. It should be noted that the reliability data presented herein represents the experience of one manufacturer of monolithic microcircuits.

C. STORAGE LIFE

The mean storage life capabilities for microcircuits, by logic family, are given in Tables 4-14 through 4-17. These data were generated from tests conducted in accordance with MIL-STD-750, Method 1031.3. Note that most of the tests were extended beyond the required 1000 hours. This was done to provide knowledge concerning extended life capabilities of microcircuits. Due to differences in structure and manufacturing techniques, the maximum storage temperature capability will vary among logic families. The storage temperature for type RCTL was +200°C, for type TTL and the linear devices it was +150°C; DTL data is supplied at both +150°C and +200°C. A composite summary of operating and storage life characteristics is given in Table 4-18. Notes which describe all observed failures are included in Table 4-18.

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Table 4-10. Operating Life Test Data Summary for Type RCTL Basic Logic Family

Item	Temperature (°C)	Number of Devices in Sample	Test Duration (Hours)	Observed Failures	Observed Test Time (Hours)
1	+125	40	4000	0	100,000*
2		40	4000	0	160,000
3		40	3000	0	120,000
4		40	3000	0	120,000
5		39	2000	1	76,500
6		39	2000	0	78,000
7		40	2000	0	80,000
8		40	2000	0	80,000
9		40	1000	0	40,000
10. Total					

	Temperature (°C)		Equivalent Total Test Time (Hours)	Failure Rate 60 Percent of Upper Confidence Limit (Percent/1000 Hours)
	Definition	Value		
11	Normal room ambient	25	7,558,200	0.013
12	Worst-case room ambient	55	5,810,600	0.035
13	Severe environment	85	2,307,150	0.097

*40 units for 2000 hours, 10 units continued for 4000 hours

Table 4-11. Operating Life Test Data Summary for Type DTL Basic Logic Family

Item	Temperature (°C)		Number of Devices in Sample	Test Duration (Hours)	Observed Failures	Observed Test Time (Hours)
1			40	2000	0	80,000
2			40	1000	0	80,000
3			40	1000	0	40,000
4	+125		40	1000	40,000	
5			40	1000	0	40,000
6			40	1000	0	40,000
7. Total			240		0	320,000
	Temperature (°C)		Equivalent Total Test Time (Hours)		Failure Rate at 60 Percent of Upper Confidence Limit (Percent/1000 Hours)	
	Definition	Value				
8	Normal room ambient	25	5,760,000		0.016	
9	Worst-case room ambient	55	2,176,000		0.042	
10	Severe environment	85	864,000		0.100	

Table 4-12. Operating Life Test Data Summary for Type TTL Basic Logic Family

Item	Temperature (°C)		Number of Devices in Sample	Test Duration (Hours)	Observed Failures	Observed Test Time (Hours)
1			39	2000	0	78,000
2			40	1500	1	58,500
3			40	1000	0	40,000
4			40	1000	0	40,000
5			40	1000	0	40,000
6			40	1000	0	40,000
7			125	1000	0	125,000
8. Total			239		1	421,500

	Temperature (°C)		Equivalent Total Test Time (Hours)	Failure Rate at 60 Percent of Upper Confidence Limit (Percent/1000 Hours)
	Definition	Value		
9	Normal room ambient	25	7,587,000	0.027
10	Worst-case room ambient	55	2,866,200	0.070
11	Severe environment	85	1,138,500	0.180

Table 4-13. Operating Life Test Data Summary for Linear Devices (Operational and Differential Amplifiers)

Item	Temperature (°C)		Number of Devices in Sample	Test Duration (Hours)	Observed Failures	Observed Test Time (Hours)
1			20	4000	0	80,000
2			20	3000	0	60,000
3			19	3000	0	57,000
4			20	2000	0	40,000
5			20	2000	0	40,000
6			20	2000	0	40,000
7			19	2000	0	38,000
8			19	2000	0	38,000
9			20	1000	0	20,000
10			20	1000	0	20,000
11. Total			197		0	433,000
	Temperature (°C)		Equivalent Total Test Time (Hours)		Failure Rate at 60 Percent of Upper Confidence Limit (Percent/1000 Hours)	
	Definition	Value				
12	Normal room ambient	25	7,794,000		0.012	
13	Worst-case room ambient	55	2,944,400		0.030	
14	Severe environment	85	1,169,100		0.080	

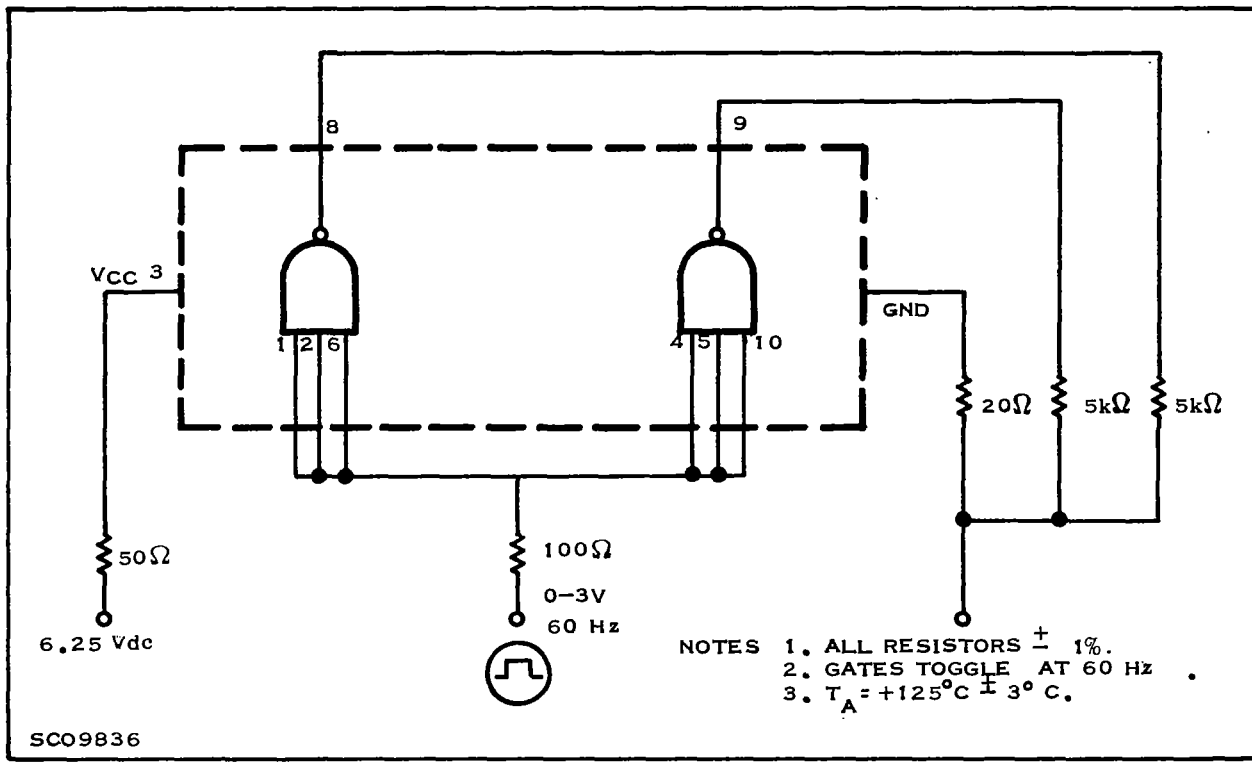


Figure 4-21. Operating Life Test Circuit (RCTL, Triple Input, Dual Gate)

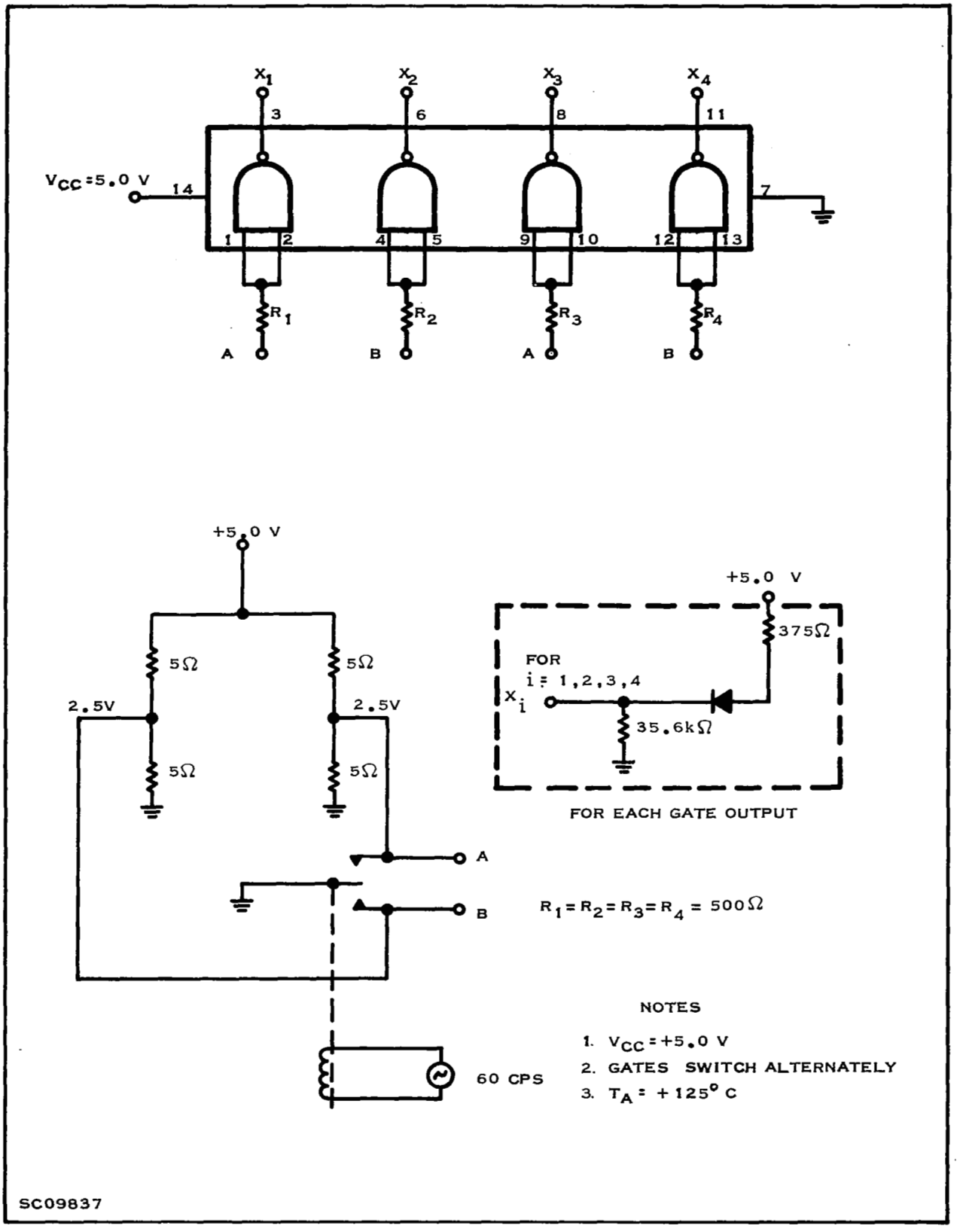


Figure 4-22. Operating Life Test Circuit (DTL, Dual Input, Quad Gate)

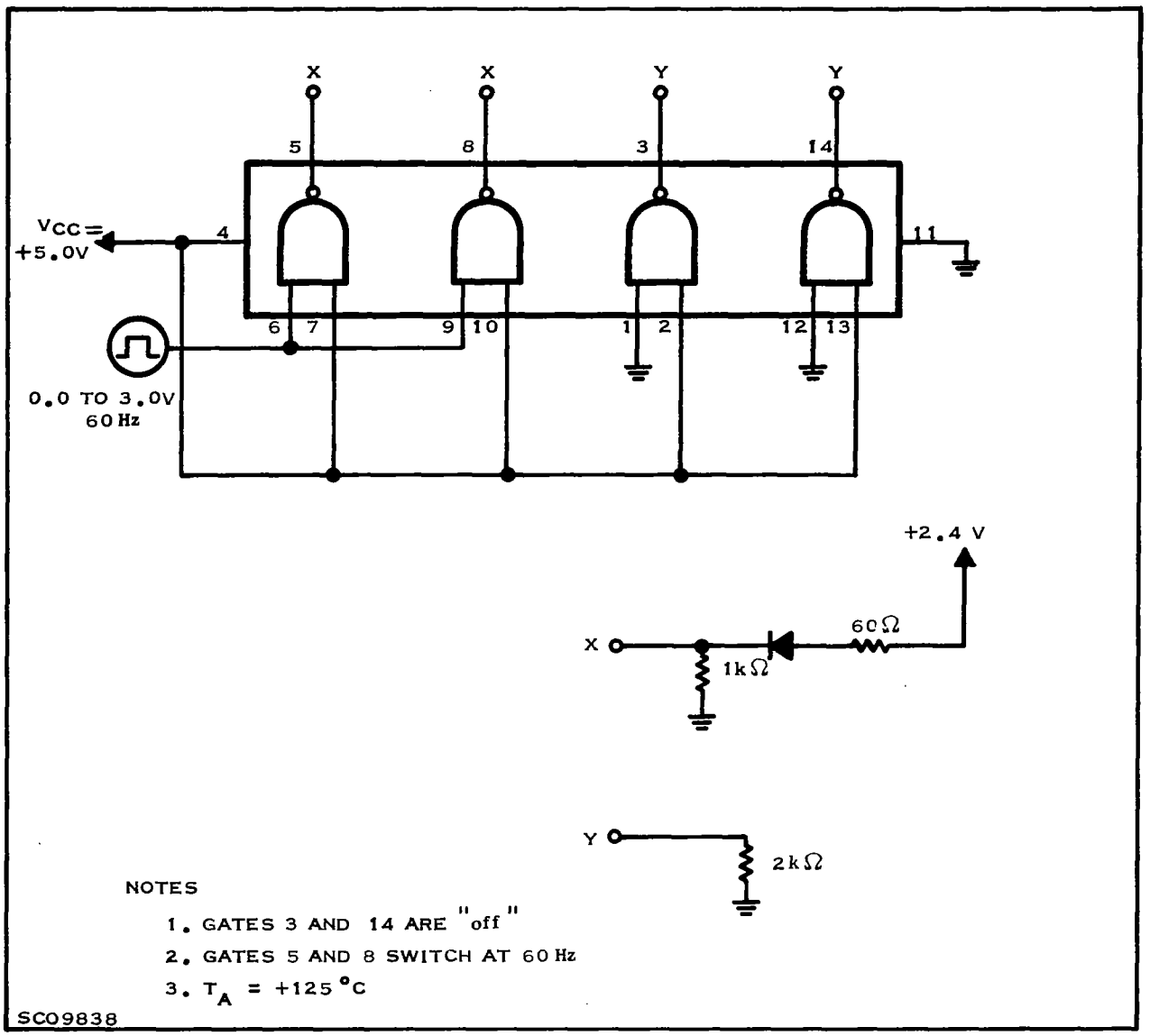


Figure 4-23. Operating Life Test Circuit (TTL, Dual Input, Quad Gate)

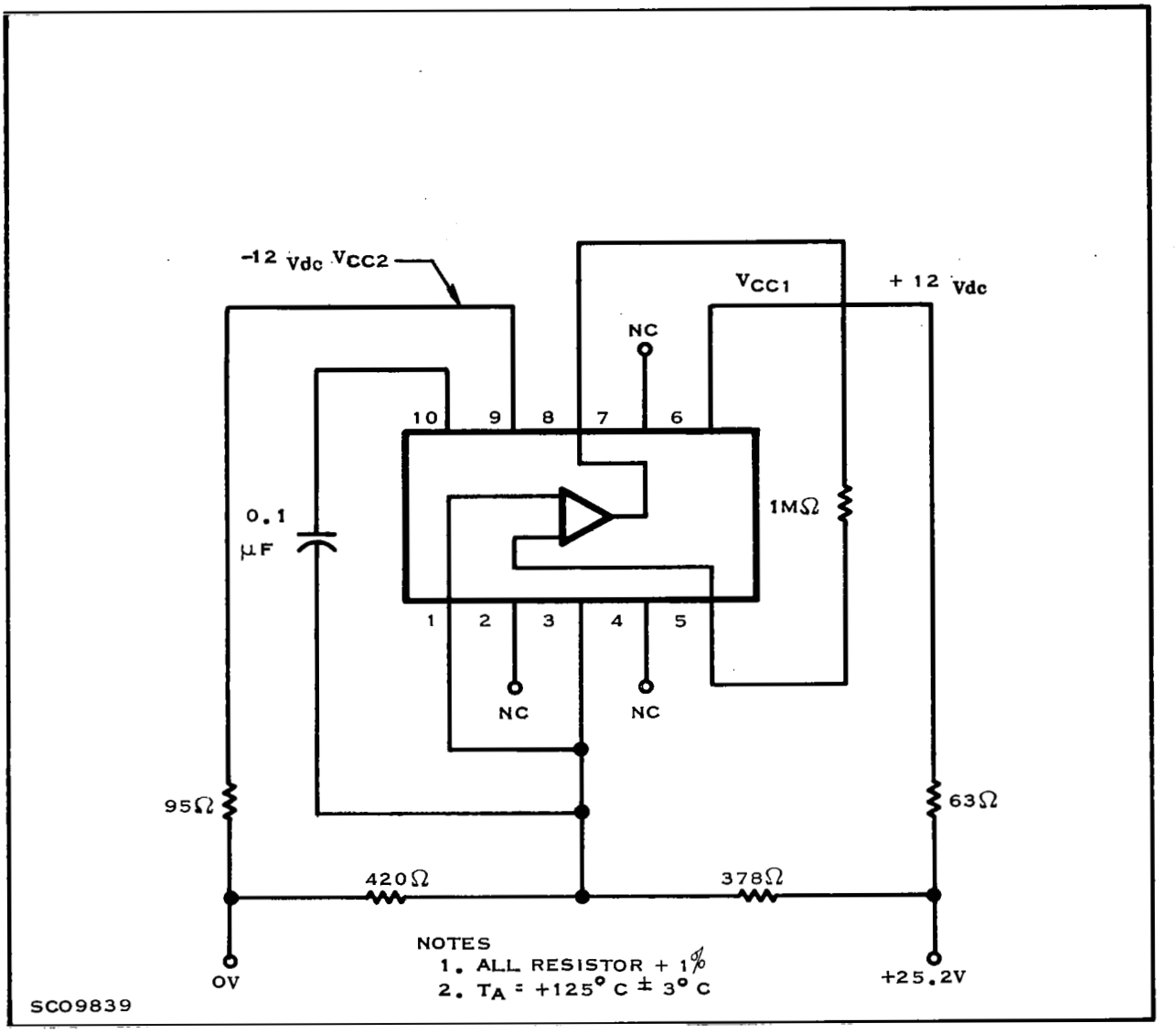


Figure 4-24. Operating Life Test Circuit (Operational Amplifier)

Table 4-14. Storage Life Test Data Summary for Type RCTL Basic Logic Family

Item	Temperature (°C)		Number of Devices in Sample	Test Duration (Hours)	Observed Failures	Observed Test Time (Hours)
1			39	5000	0	185,000
2			39	4000	0	156,000
3			40	4000	0	160,000
4			40	3000	0	120,000
5	+200		38	2000	0	76,000
6			40	2000	0	80,000
7			40	2000	0	80,000
8			39	1000	0	39,000
9			39	1000	0	39,000
10. Total			354		0	935,000
	Temperature (°C)		Equivalent Total Test Time (Hours)		Failure Rate at 60 Percent of Upper Confidence Limit (Percent/1000 Hours)	
	Definition	Value				
11	Normal room ambient	25	46,750,000		0.002	
12	Worst-case room ambient	55	17,484,500		0.005	
13	Severe environment	85	7,012,500		0.013	

Table 4-15. Storage Life Test Data Summary for Type DTL Basic Logic Family

Item	Temperature (°C)	Number of Devices in Sample	Test Duration (Hours)	Observed Failures	Observed Test Time (Hours)
1		40	2000	0	80,000
2		40	2000	0	80,000
3	+150	40	2000	1	80,000
4		40	2000	0	80,000
5. Subtotal		160		1	320,000
6		40	2000	0	80,000
7	+200	40	2000	0	80,000
8		38	1000	0	38,000
9. Subtotal		118		0	198,000
10. Total		278		1	518,000

	Temperature (°C)		Equivalent Total Test Time (Hours)	Failure Rate at 60 Percent of Upper Confidence Limit (Percent/1000 Hours)
	Definition	Value		
11	Normal room ambient	25	17,804,000	0.010
12	Worst-case room ambient	55	6,262,600	0.030
13	Severe environment	85	2,669,000	0.076

Table 4-18. Composite Summary of Operating and Storage Life Capabilities of Principal Basic Logic Families of Monolithic Microcircuit Devices

Item	Monolithic Microcircuit Device (Basic Logic Family)	Observed Test Time (Hours)	Observed Device Failures	Equivalent Test Temperature and Time		Failure Rate at 60 Percent of Upper Confidence Limit (Percent/1000 Hours)
				Temperature (°C)	Time (Hours)	
1	RCTL	1,789,500	1[a]	25	62,131,000	0.003
2				55	23,294,600	0.009
3				85	9,319,650	0.022
4	DTL	838,000	1[b]	25	23,564,000	0.009
5				55	8,438,600	0.024
6				85	3,533,000	0.057
7	TTL	611,500	1[c]	25	15,367,500	0.013
8				55	5,386,200	0.0389
9				85	2,304,000	0.09
10	Linear	739,000	1[d]	25	15,352,200	0.013
11				55	5,392,400	0.037
12				85	2,301,300	0.088
13. Total		3,978,000	4			
14. Total	All families			25	116,414,700	0.0044
15. Total				55	42,511,800	0.0115
16. Total				85	17,457,950	0.0300

Note	Cause of Failure	Corrective Action Taken
a	One unit failed after 1000 hours of operating life. Cause of failure was an oxide defect.	Conversion to post emitter oxide (900°C steam) should have a major impact on reducing this failure mechanism.
b	One unit failed after 2000 hours of storage life at 150°C. Cause of failure was an extraneous wire in the package that caused an internal short circuit condition.	Visual escape - QC performs lot acceptance after pre-cap and bar inspection to control visual escapes. Lot rejections and percent defective are monitored by QC and Engineering personnel to implement improvements on a continuing basis.
c	One unit failed after 1000 hours of operating life. Cause of failure was improper bond placement.	Installation of bond temperature and capillary weight surveillance, and a new bond shear strength surveillance.
d	One unit failed after 2000 hours of storage life at 150°C. Cause of failure was improper bonding procedure.	Installation of bond temperature and capillary weight surveillance, and a new bond shear strength surveillance.

SECTION V

ENVIRONMENTAL CAPABILITIES

A. GENERAL

Because of their size and weight advantages, monolithic microcircuits have found wide acceptance in space, military, and avionics programs. Inherent in these applications are many varied environmental conditions that can have significant impact on reliability. Long life is not sufficient, a product must also be capable of withstanding the sudden and sustained acceleration forces encountered in "lift off," catapult launches from a carrier, etc. Vibrations at various frequencies and sudden shocks are also encountered. Other stresses likely to be encountered are rapid temperature fluctuations, conditions of high humidity and salt atmosphere.

This section contains data obtained from a series of environmental step-stress tests performed on the RCTL, DTL, TTL, and linear families of monolithic microcircuits. The discussion is presented in two parts–mechanical tests and thermal-moisture tests. The test results show that monolithic microcircuits are capable of passing environmental stress levels far in excess of those specified for military and space applications.

B. MECHANICAL STRESS

1. General

Mechanical stressing is performed to insure that components have the capabilities to withstand: sudden changes in applied force, rough handling and sustained acceleration forces of a large amplitude. Failure modes most susceptible to detection by mechanical stressing are:

- Weak or intermittent bonds.
- Cracks in the silicon die (chip).
- Excessively long or misplaced lead wires that are subject to electrical shorting.
- Foreign particles in the package that can possibly cause opens or shorts.
- Inadequate silicon die support.

2. Method of Testing

Testing was conducted using the step-stress method. Descriptions of the individual tests performed are as follows:

- Shock. Each device was subjected to five blows in each of four planes (X_1, Y_1, Y_2, Z_1) for a total of twenty blows. The units were tested at the following three consecutively higher levels of shock:
  - 1500 G–0.5 ms duration
  - 3000 G–0.5 ms duration
  - 4000 G–0.2 ms duration
- Vibration, Variable Frequency. Each device was subjected to four sweeps in each of three mutually perpendicular planes (X_1, Y_1, Z_1). One sweep consisted of traversing the frequency range of 100 to 2000 Hz and return to 100 Hz in four minutes. Testing was conducted at the following levels of constant peak acceleration:
  - 20 G
  - 30 G
  - 50 G
- Constant Acceleration. Each unit was subjected to one minute of time of sustained acceleration in each of three mutually perpendicular planes (X_1, Y_1, Z_1). Testing was conducted at the following levels of acceleration:
  - 20,000 G
  - 35,000 G
  - 50,000 G

3. Test Results

Test results for the RCTL, DTL, TTL, and Linear families are summarized in Table 4-19.

C. THERMAL-CHEMICAL STRESS

1. General

Tests in this category are conducted in order to determine the ability of components to withstand high humidity and corrosive (sea coast) environments and sudden, extreme changes in temperatures. Failure mechanisms most susceptible to detection by this type of testing are:

- Lack of package hermeticity.
- Cracks in the silicon die (chip).
- Weak glass-to-metal seals.
- Intermittent contacts in the surface metallization system.
- Weak or intermittent bonds.

Table 4-19. Summary* of Mechanical Stress Tests of Basic Logic Device Families

Test	Test Level (G)	RCTL		DTL		TTL		LINEAR	
		Tested	Failed	Tested	Failed	Tested	Tailed	Tested	Failed
Shock	1,500	20	0	20	0	20	0	20	0[e]
	3,000	20	0	20	0	20	0	19	0
	4,000	20	0	20	0	20	0	19	0
Vibration, Variable Frequency	20	20	0	20	0	20	0	20	0
	30	20	0	20	0	20	0	20	1[f]
	50	20	0	20	0	20	0	19	0
Constant Acceleration	20,000	20	0	70	2[a]	18	0	20	0[g]
	35,000	20	0	19	3[b]	18	0	18	0
	50,000	20	0	16	2[c]	18	1[d]	18	0

* Based on Tests conducted during third and fourth quarters of 1966.

Note	Cause of Failure	Corrective Action Taken
a	One unit—failed due to pitted gold wire near stitch bond	This may be considered a random escape from incoming quality control (QC) inspection. It was the first failure of its type observed by one manufacturer in over 5 years of testing microcircuits. Since it was an exceptional failure it is not considered to represent a reliability risk.
	One unit—undetermined (possible test error)	None possible.
b	One unit—sagging gold wire shorted out	Redesigned package to move external leads closer to silicon die.
	One unit—undetermined	None possible.
	One unit—"pigtail" on an external pin tab bond shorted to case.	Implemented a "pigtail remover" on bonding machine.
c	Two units—pinched wire	Implemented bonder surveillance along with bond temperature and capillary weight surveillance.
d	One unit—sagging gold wire shorted out	Redesigned package to move external leads closer to silicon die.
e	One unit—unit electrically overstressed by test set	More advanced test equipments are being studied to improve test capability.
f	One unit—crack in silicon die	Implemented a requirement for 75 percent coverage of pyroceram.
g	Two units—were incorrectly mounted in test fixture and destroyed	None possible.

2. Method of Testing

Testing was conducted using the step-stress method. Descriptions of the individual tests performed are as follows:

- Thermal shock. Each unit was subjected to the specified temperature extremes for fifteen seconds of time, with a three-second maximum transfer time between the temperature extremes. Specified temperatures and number of cycles were as follows:
  - 0°C to 100°C, 5 cycles
  - -55° C to +150° C, 40 cycles (45 total)
- Temperature Cycling. One cycle consisted of storing the unit for fifteen minutes at each temperature extreme; the maximum transfer time was five minutes (at 25° C). Specified temperatures and number of cycles were as follows:
  - -65° C to +125° C, 10 cycles
  - -65° C to +125° C, 40 cycles (50 total)
- Moisture Resistance. The units were tested in accordance with MIL-STD-202C, Method 106B. The units were nonoperating and the initial preconditioning was omitted. Length of testing was as follows:
  - 10 cycles
  - 20 cycles (30 cycles total)
- Salt Atmosphere. The units were subjected to a salt atmosphere fog having a temperature of 35°C and a salt deposit rate of between 10,000 to 50,000 $mgm/m^2/day$. Test duration was as follows:
  - 24 hours
  - 24 hours (48 hours total)

3. Test Results

Test results for the RCTL, DTL, TTL and Linear families are summarized in Table 4-20. The salt atmosphere avaluation is primarily a test of the package and not the particular logic function. For this reason, salt atmosphere data was accumulated on the RCTL family only.

Table 4-20. *Summary of Thermal-Chemical Stress Tests of Basic Logic Device Families

Test	Test Level	RCTL		DTL		TTL		LINEAR	
		Tested	Failed	Tested	Failed	Tested	Failed	Tested	Failed
Thermal Shock	1. 5 cycles	20	0	20	0	20	2[a]	20	0[b]
	2. 40 cycles	20	0	20	0	18	0	19	0
	(45 total)								
Temperature Cycling	1. 10 cycles	20	0	20	0	20	0	20	0
	2. 40 cycles	20	0	20	0	20	0	20	0
	(50 total)								
Moisture Resistance	1. 10 days	20	0	20	0	20	0	20	0
	2. 20 days	20	0	20	0	20	0	20	0
	(30 total)								
Salt Atmosphere	1. 24 hours	20	0						
	2. 24 hours	20	0						
	(48 total)								

*Data on salt atmosphere tests was generated during first quarter of 1966. All other data came from test conducted during third and fourth quarter of 1966.

Note	Cause of Failure	Corrective Action Taken
a	One unit failed due to cracked bar	Implemented a requirement for 75 percent coverage of pyroceram in conjunction with the usage of alumina filler in the pyroceram.
	One unit failed due to internal contamination by residue from a production process	Installed improved wash process and implemented tighter visual inspection criteria.
b	One unit was electrically overstressed by test set.	More advanced test equipments are being studied to improve test capability.

SECTION VI

SEVERE OVERSTRESS CAPABILITIES

A. GENERAL

A key factor to reliability improvement lies in a manufacturer's ability to analyze reliability failures, detect and identify the failure mechanisms and cycle this information back to the design and manufacturing areas for definitive corrective actions. However, this procedure is predicated upon first generating failures; and, as can be seen from the data presented in Section IV (mean life characteristics), normal life tests, even at maximum rated conditions, do not generate a sufficient number of failures for this purpose. There are, then, two alternatives: either test more devices or use accelerated stress levels. In the interests of both time and monetary savings, the latter approach is the more practical of the two.

The underlying assumption in overstress testing (commonly called stress testing) is that time, temperature, and power-related failure mechanisms can be accelerated by increasing the stress level in discrete steps until failure occurs. Analysis of units that failed will yield valuable information about failure mechanisms and give clues as to the specified areas that need corrective action.

The step-stress tests presented here fall into two categories: 1) power step stress where the units are operated for specific time intervals as successively increasing power levels, and 2) temperature step stress where the units are stored at successively higher temperature levels for discrete periods of time.

B. POWER STEP STRESS

This discussion of power step stress presents the results of recent tests conducted on a six-input NAND/NOR gate from the RCTL family. The RCTL family is characteristic of microcircuits that have very low-power dissipation levels. The test was designed to deliberately induce, at high-power levels, electrical degradation of the transistor junctions. Although the test did not generate any failures, it is significant to note that the devices are capable of dissipating nearly one watt of power for four continuous hours of operating time without failing. The test sequence and results are summarized in Table 4-21.

C. Temperature Step Stress

The purpose of temperature-step-stress testing is to accelerate temperature-dependent failure mechanisms. In addition to the knowledge gained from an analysis of the failures, the test results can be used to make comparisons between samples manufactured at different times to determine if

Table 4-21. Summary of Power Step Stress Test

Step (Time per step = 4 hours)	V_{cc} (Volt, dc)	I_j per input (mA)	ΣI_j per device (mA)	Power Dissipation (mW)	Devices Tested	Failures
1	+6.0	12.5	75.0	450	30	0
2	+6.0	15.3	92.0	550	30	0
3	+8.0	13.5	81.0	650	30	0
4	+8.0	15.6	94.0	750	30	0
5	+8.0	17.6	106.0	850	30	0
6	+8.0	19.8	119.0	950	30	0

the relative thermal strength of the microcircuits is remaining constant, improving, or degrading with time. The test sequence and results are summarized in Table 4-22.

A plot of failure distribution data from the temperature step stress test for a TTL family of devices is shown in Figure 4-25. These devices were manufactured using a gold-aluminum metallization system, which is susceptible to the formation of intermetallic compounds at high temperature. The RCTL and DTL units evaluated were monometallic gold metallization. Because of this distinction, the failure distribution of TTL devices is different from that of the RCTL and DTL families. Temperature-step-stress failure distribution data for the linear device family is shown in Figure 4-26. A summary of data from temperature-step-stress tests performed on the RCTL, DTL and linear families of monolithic microcircuits is shown in Table 4-22.

Table 4-22. Summary of Temperature-Step-Stress Tests Performed on the RCTL, DTL, TTL and Linear Families of Monolithic Microcircuits

Monolithic Microcircuit Device (Basic Logic Family)	Step n = 20 (Time per step = 4 hours)	Temperature (°C)	Failures	Cumulative Failures	Cumulative Percent of Failures
RCTL	1	200	0	0	0
	2	250	0	0	0
	3	300	0	0	0
	4	350	0	0	0
	5	375	0	0	0
	6	425	2*	2	10
	Step n = 20 (Time per step = 4 hours)				
DTL	1	200	0	0	0
	2	250	0	0	0
	3	300	0	0	0
	4	350	0	0	0
	5	375	0	0	0
	6	425	0	0	0
	Step n = 20 (Time per step = 4 hours)				
TTL	1	200	0	0	0
	2	250	1	1	5
	3	300	12	13	65
	4	350	5	18	90
	5	375	0	18	90
	6	425	2	20	100
	Step n = 20 (Time per step = 4 hours)				
Linear	1	200	0	0	0
	2	250	0	0	0
	3	300	1	1	5
	4	350	1†	2	10
	5	375	1†	3	15
	6	425	2†	5	25

*Failure analysis of these two units revealed the cause of failure to be gold migration into the silicon. Failures of this type are to be expected when the units are stressed above the 377°C gold-silicon eutectic point.

†At temperatures above 300°C, device failures are attributable to the formation of AuAl intermetallic compounds.

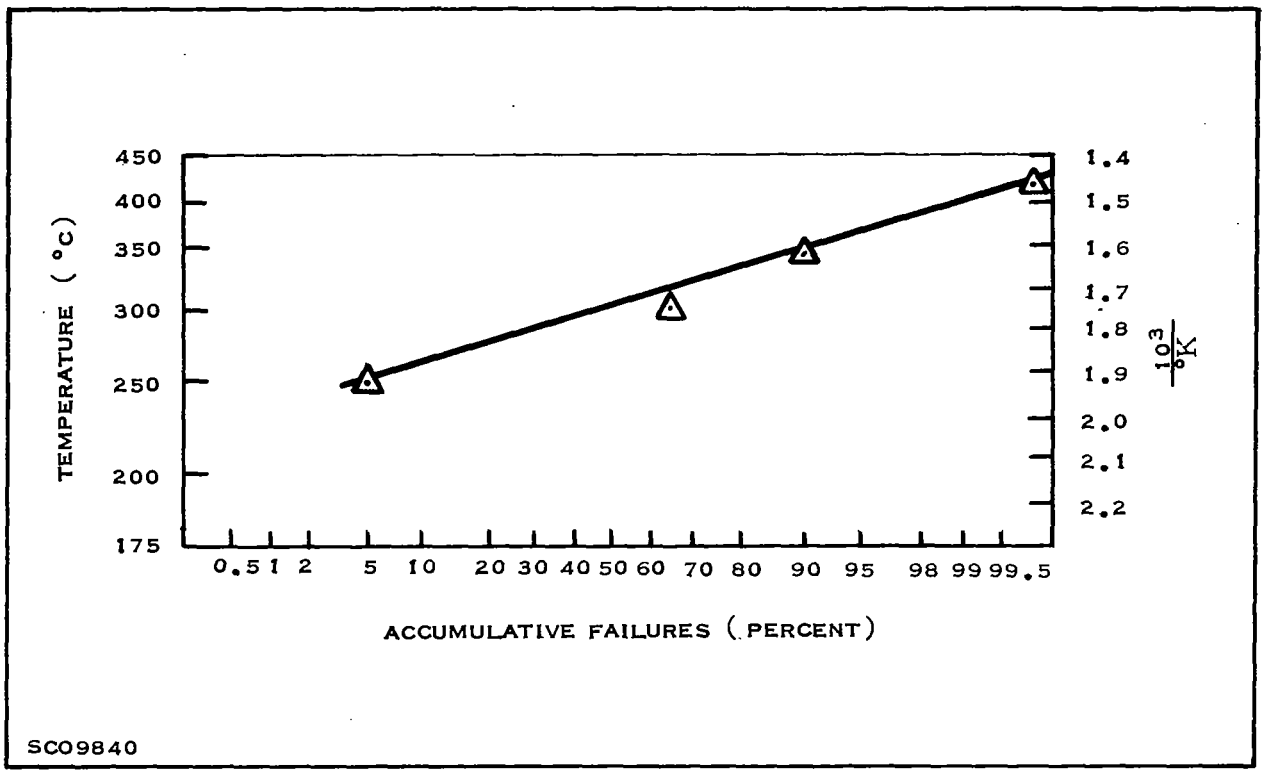


Figure 4-25. Temperature Step Stress Test (TTL Device Family Failure Distribution

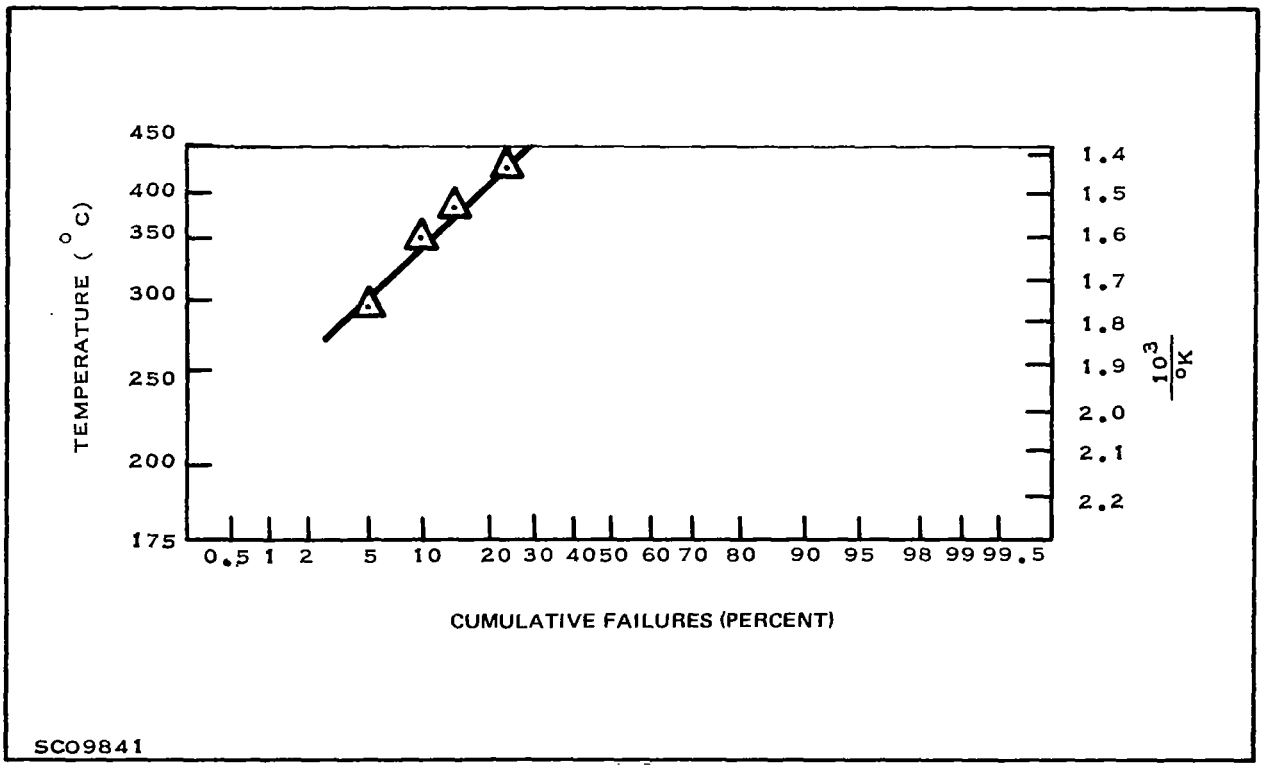


Figure 4-26. Temperature Step Stress Test (Linear Device Family Failure Distribution

SECTION VII

PARAMETER STABILITY

A. GENERAL

Electrical parameter stability of components is a major concern for a system design engineer. Should one component of a system or sub-system fail to perform within its required design tolerance, the results may jeopardize the mission success of that system. Therefore the system designer must be familiar with the stability characteristics of each component used.

Parameter drift may be accelerated and therefore used as a screening mechanism for potentially unreliable components. However, a mechanism of this nature is practical only when applied to those selected parameters which are most sensitive to the system design.

An analysis of microcircuits parameter stability is given below. This analysis will cover both digital and linear circiuits and was performed on data obtained from reliability evaluation tests of "off-the-shelf" devices that had received no special screening or preconditioning. Hence the data herein can be taken to represent a truly worst-case estimate of parameter stability.

B. DIGITAL CIRCUITS

1. Basic Considerations of the Causes of Parameter Drift

All components are subject to physical and/or electrical deterioration during operation. This deterioration will cause parameter drift. This deterioration, and the resultant drift, can be accelerated by the following methods:

- Operating devices at high temperature (i.e., at +156°C) for sustained periods of time.
- Subjecting devices to extremely high temperatures (over 200° C), in discrete steps, for short time periods.
- Operating devices at elevated power levels (ambient temperature held constant).
- Subjecting devices to a high-humidity so as to promote the penetration of moisture into the package.

2. Procedure for Analysis of Parameter Stability

The process of analyzing parameter stability began with the selection of representative test samples from each of the categories in the preceding list. The only criteria used in selecting the samples was that they consist of the same or similar device types. This was done for two reasons:

first, it simplified data handling, collection, and analysis; secondly it afforded an opportunity to compare the results between tests (i.e., temperature step stress versus power step stress, etc.) and to analyze the results of the individual tests.

The analysis involved the use of the normal distribution equations discussed in Section II-B, Part 5. Recall that the mean (μ) and standard deviation (σ) of a normal population are defined as:

$$\mu \simeq \bar{x} = \frac{1}{n} \sum_{i=0}^{n} x_i \tag{22}$$

$$\sigma \simeq \bar{s} = \sqrt{\frac{\sum_{i=1}^{n} (\bar{x} - x_i)^2}{n - 1}} \tag{23}$$

Using these relationships, the mean and standard deviation values for V_{on} (logical "O" voltage output level, V_{off} (logical "1" voltage output level and I_{in} (input current) were calculated for the initial and all post-stress measurements. The μ and $\pm 2\sigma$ values were plotted versus time/stress level in order to show any apparent trends in parameter behavior. The $\pm 2\sigma$ limits were used in lieu of the 1σ limits because the former incorporate approximately 95 percent of the total population.

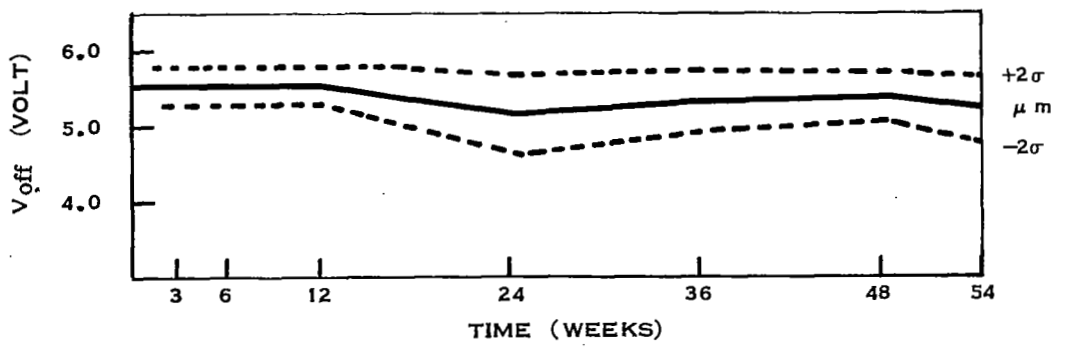
3. Results of Parameter Stability Analysis

The results of the parameter stability analysis are shown in Figures 27 to 30. The graphs show excellent parameter stability of the units under all four stress conditions. The temperature-step-stress test indicated the greatest amount of parameter drift between the initial and last steps. The I_{in} mean changed from 44 μA to 40 μA, or approximately a 10 percent change; V_{on} increased by approximately the same amount. It should be noted, however, that the parameters held stable up to the 375° C stress level, which is near the gold-silicon eutectic point of 377°C. When stressing above this level it is possible to create catastrophic failure due to gold-silicon interaction.

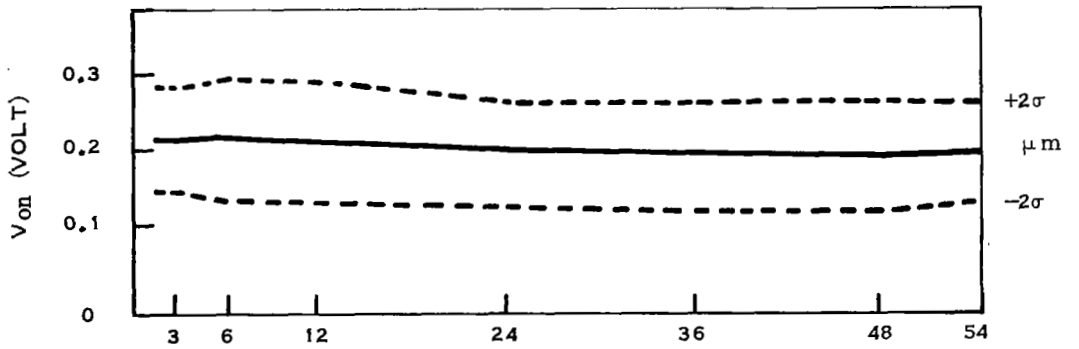
C. LINEAR CIRCUITS

The analysis of linear circuits did not focus upon the same characteristics as were considered in the discussion of digital circuits. The need for V_{on} and V_{off} stability is obvious, since these parameters are a direct indicator of a digital device's ability to perform its basic switching function. Also input current, I_{in}, is an important consideration when devices are being operated at or near their maximum rated fan-out loads. These considerations are not applicable to linear circuits since their basic function is to amplify incoming signals, we are primarily concerned with gain. We define amplifier gain (A_G) as the ratio of voltage out to voltage in, or:

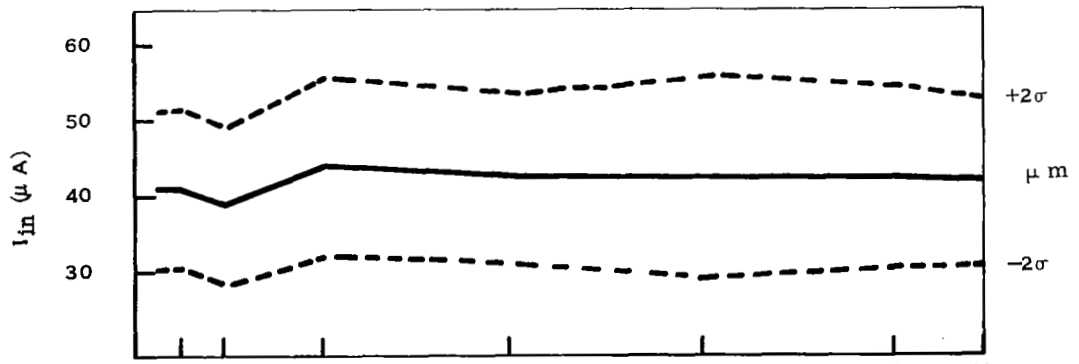
$$A_G = \frac{V_{out}}{V_{in}} \tag{24}$$



(A) V_{off} VOLTS (LOGICAL "ONE" VOLTAGE OUTPUT LEVEL, N=0)



(B) V_{on} VOLTS (LOGICAL "ZERO" VOLTAGE OUTPUT LEVEL)



(C) I_{in} A INPUT CURRENT

NOTES: T_A = +125 °C
V_{CC} = + 6.0 V
SAMPLE SIZE = 10

SC09847

Figure 4-27. Extended Operating Life Test, Mean and Standard Deviation Values (RCTL, Six-Input NAND/NOR Gate)

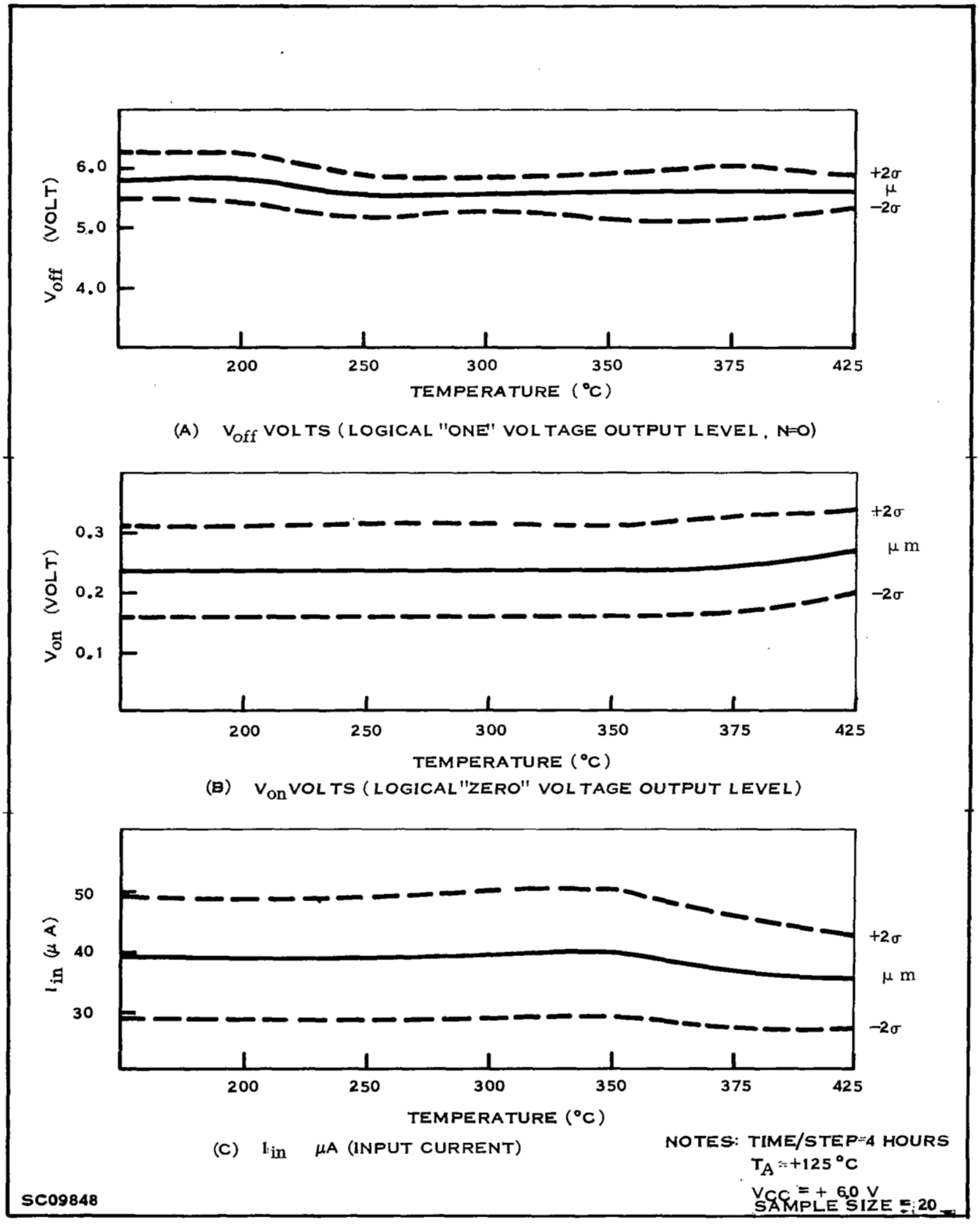
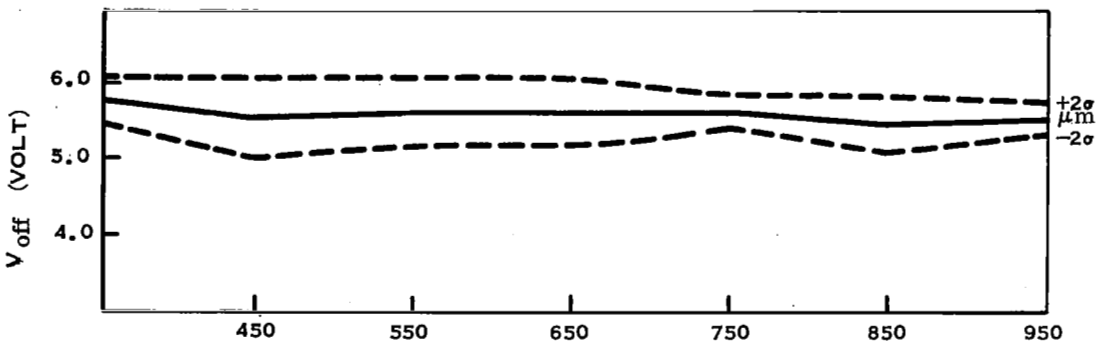
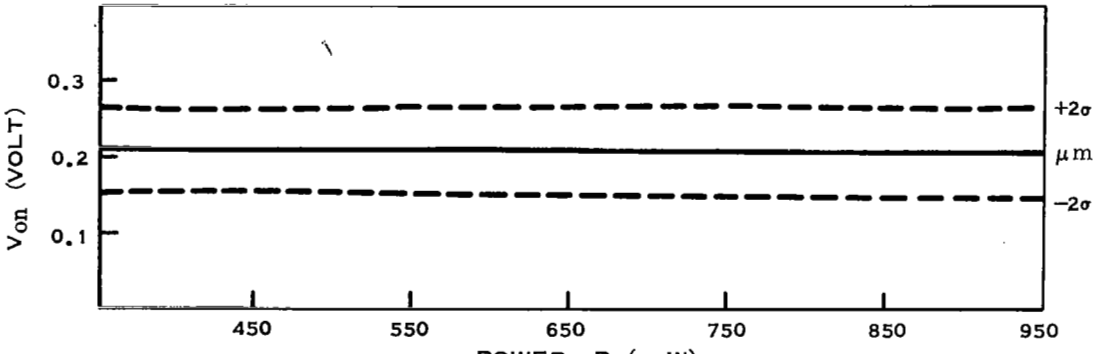


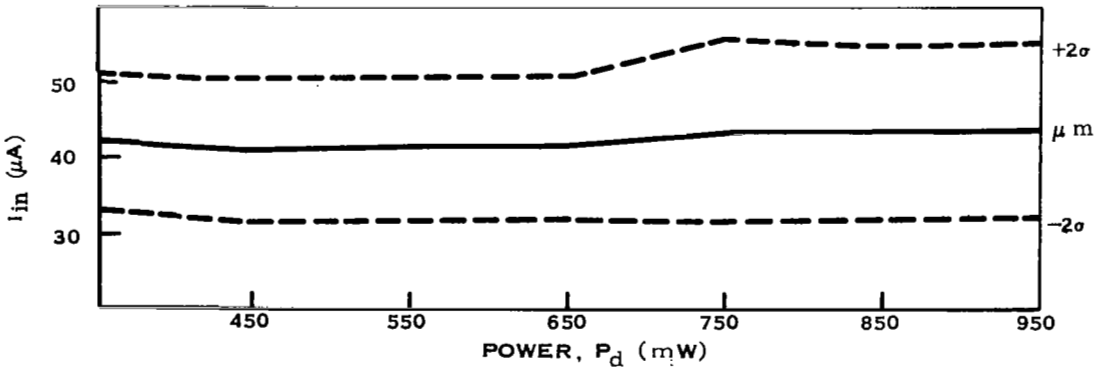
Figure 4-28. Temperature Step Stress Test, Mean and Standard Deviation Values (RCTL, Six-Input NAND/NOR Gate)



(A) V_{off} VOLTS (LOGICAL "ONE" VOLTAGE OUTPUT LEVEL, NO)



(B) V_{on} VOLTS (LOGICAL "ZERO" VOLTAGE OUTPUT LEVEL)

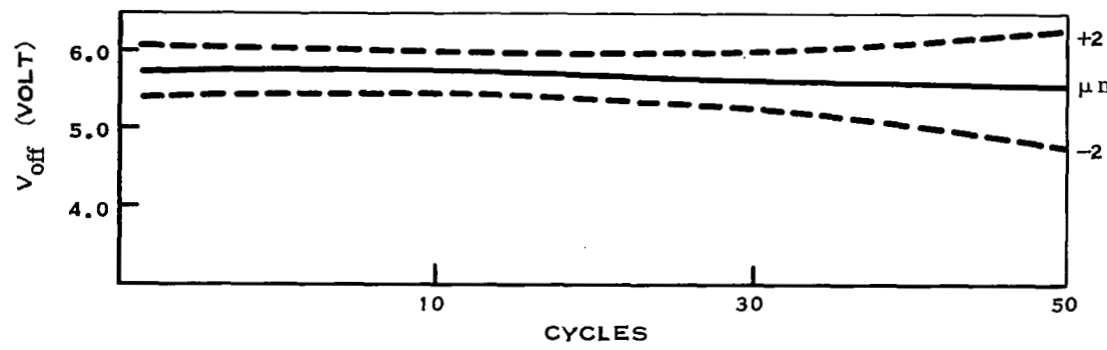


(C) I_{in} A (INPUT CURRENT)

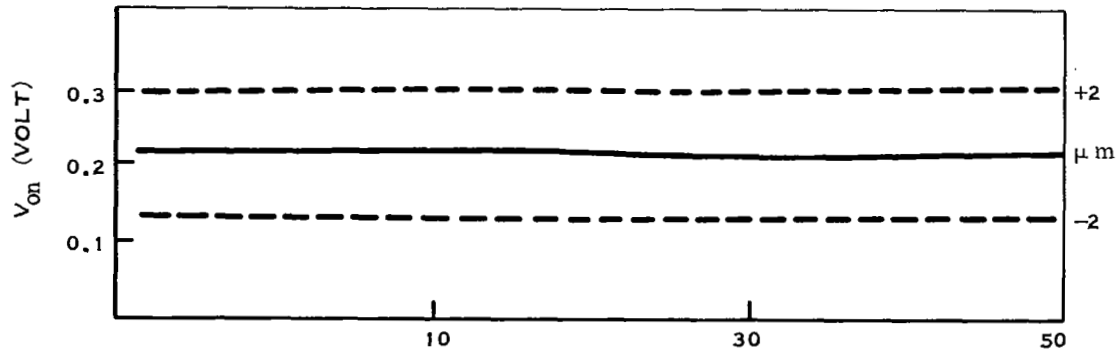
NOTES TIME/STEP = 4 HOURS
T_A = +125°C
V_{CC} = +6.0 V
SAMPLE SIZE = 20

SC09849

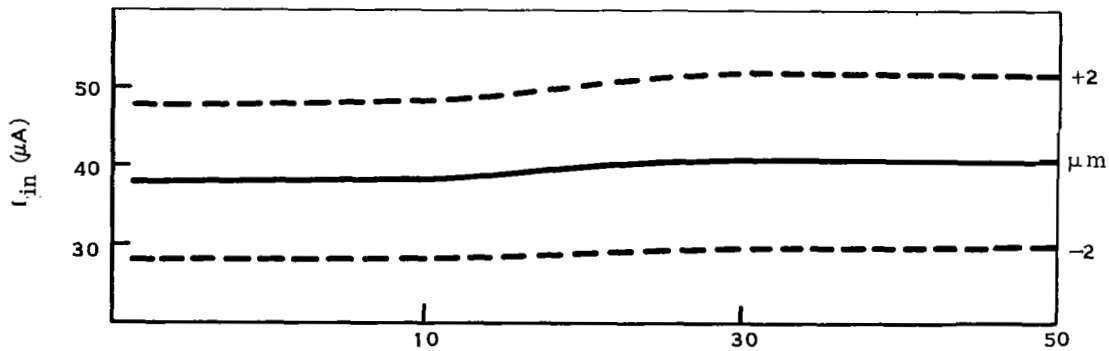
Figure 4-29. Operating Step Stress Test, Mean and Standard Deviation Values (RCTL, Six-Input NAND/NOR Gate)



(A) V_{off} VOLTS (LOGICAL "ONE" VOLTAGE OUTPUT LEVEL, N=O)



(B) V_{on} VOLTS (LOGICAL "ZERO" VOLTAGE OUTPUT LEVEL)



(C) I_{in} A (INPUT CURRENT)

NOTES T = +125 °C
V_{CC} = +6.0 V
SAMPLE SIZE = 20

SC09850

Figure 4-30. Moisture Resistance, Mean and Standard Deviation Values (RCTL, Dual Three-Input NAND/NOR Gate)

This discussion will use "scatter plots" to demonstrate gain stability with respect to operating life at elevated temperatures. These plots, shown in Figures 4-31 and 4-32, have identical scales on both the vertical and horizontal axes. The data points are of the form $P_i (X_i, Y_i)$, where X_i and Y_i are the initial and post-stress parameter values of the i^{th} device. Data for units with 0 percent change between pre-and post-readings will plot on a line drawn from P(0,0) at a 45° angle (i.e., a line with a slope of unity). Hence the more nearly the data points are clustered about the reference line, the better the parameter stability of the population. The scatter plots shown in Figures 4-31 and 4-32 were constructed from linear operational amplifier data gathered from operating life tests conducted in 1966.

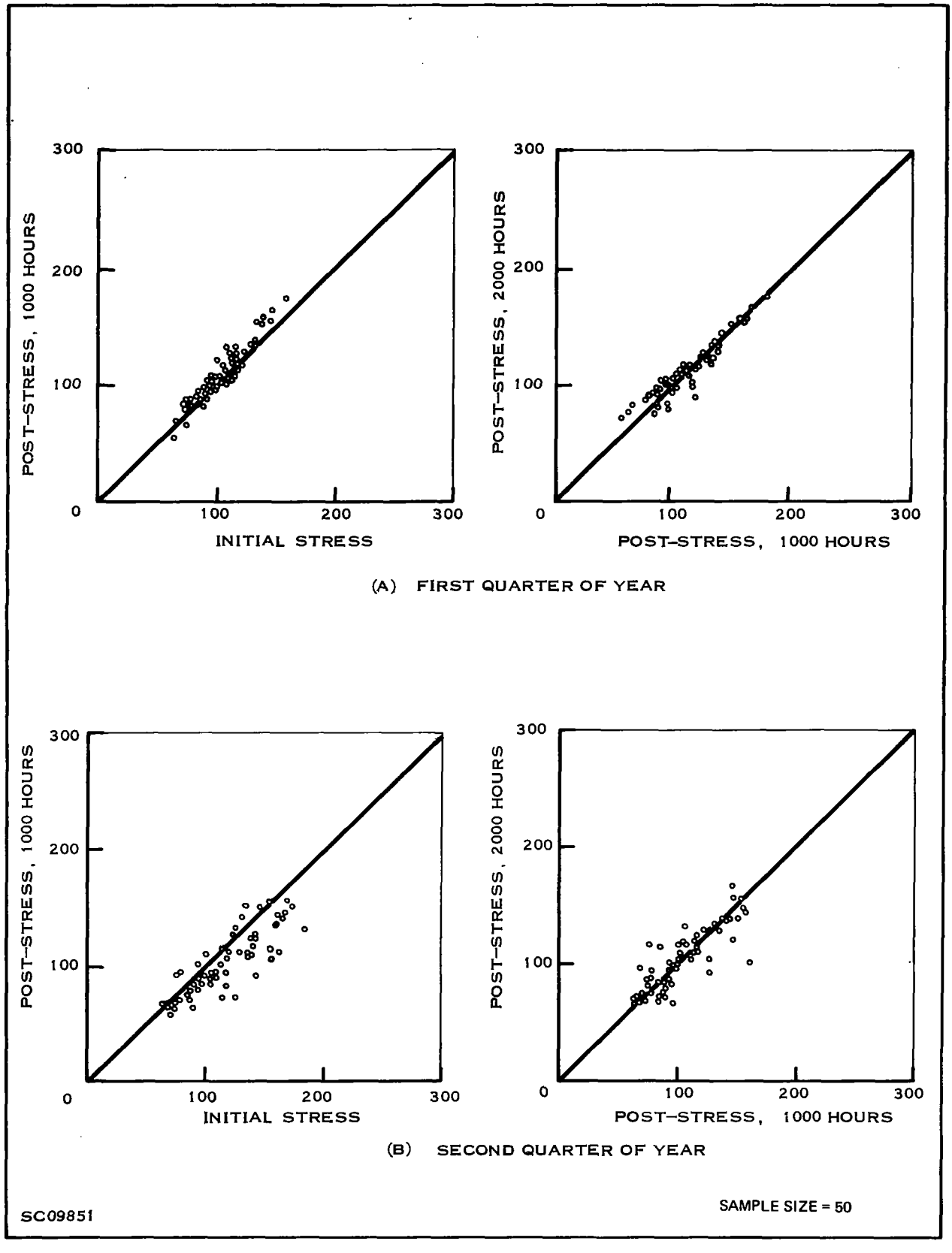
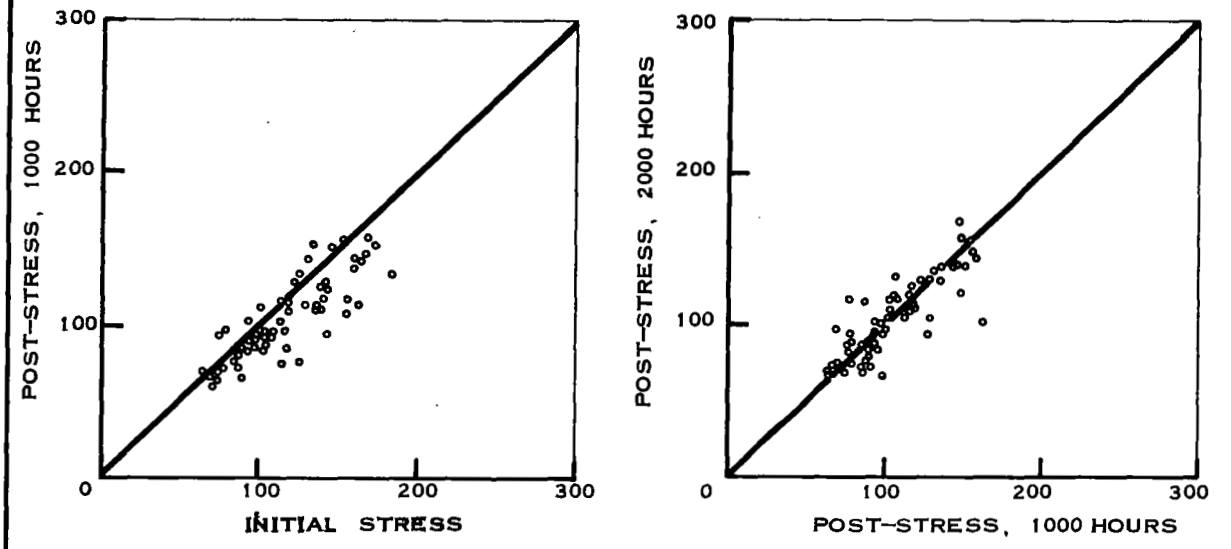
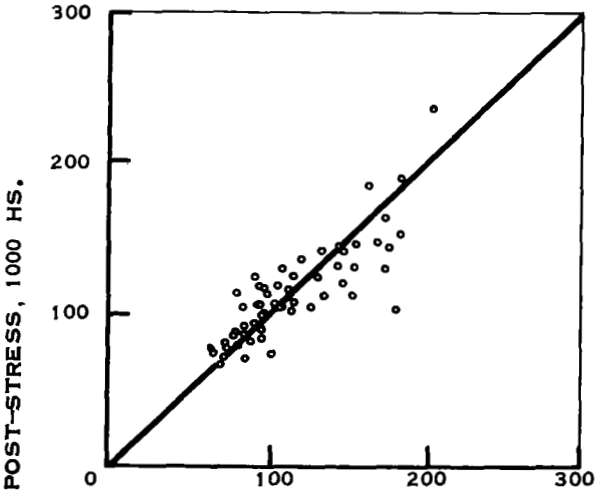


Figure 4-31. Voltage Gain (· 10) Stability of Linear Operational Amplifier with Respect to Operating Life at Elevated Temperatures (Sheet 1 of 2)



(C) THIRD QUARTER OF YEAR

NOTE: FOURTH QUARTER LIFE TESTS HAVE NOT COMPLETED 2000 HOURS AT TIME OF PUBLICATION.



(D) FOURTH QUARTER OF YEAR

SAMPLE SIZE = 50

SC09852

Figure 4-32. Voltage Gain (· 10) Stability of Linear Operational Amplifier with Respect to Operating Life at Elevated Temperatures (Sheet 2 of 2)

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